DRIFTING-DIPOLE NOISE MODEL OF NANOMETER MOSFETS FOR RADIO FREQUENCY INTEGRATED CIRCUIT DESIGN

BY

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DISSERTATION

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ABSTRACT

Recent advances in nanometer CMOS scaling technology have made transistors capable of operating at hundreds of gigahertz, and opened a new era of high performance, low cost system-on-chip (SOC) designs for multi-gigabit-per-second wireless communication. However, such achievements also bring new challenges, particularly in modeling the physical behaviors of these super-scaled devices. Among these issues, it is found that the thermal-noise based formulation, such as the one in the widely accepted BSIM model, starts to deviate from the measured noise parameters of 120-nm CMOS devices. Therefore a new high-frequency noise model is required to allow first-pass radio frequency integrated circuit (RFIC) designs using state-of-the-art CMOS technologies.

As the MOSFET is scaled down, the lateral field across the device channel becomes comparable to, or even exceeds, the vertical field. The device can no longer be considered as operating under equilibrium condition, and the thermal noise theory is no longer applicable to predicting its performance. This work describes a new noise formulation that takes into account high-field effects by using the concept of unrelaxable drifting dipoles. The proposed noise model is verified for single devices as well as for integrated circuits. Excellent fitting results are achieved for the measured noise parameters of single 120-nm MOSFETs. For circuit validation, two high-performance low-noise amplifiers (LNA) have been demonstrated. The 3.1–10.6 GHz Ultra Wideband LNA shows very low noise figures *NF* of 3.5 to 4.3 dB as well as superior input-referred third-order interception points IIP_3 of 3.5 to 5.2 dBm across the design bandwidth. The other circuit, a 24-GHz LNA, achieves a gain of 19 dB, the highest gain published to date at this frequency band, while maintaining a comparative noise figure *NF* of 3.8 dB.

To my family

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This work would not have been possible without the help of the many people with whom I have been fortunate to have been associated.

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1. INTRODUCTION

1.1 Noise and Dynamic Range of Electronic Circuits

Dynamic range (DR) is an important concept in RF or mixed signal circuit design. It indicates the input power ranges which the input signal can be well detected and the circuit can be used without significant degradation of signal quality (Figure 1.1). The upper bound is typically limited by the nonlinearity (1 dB compression point, IP1dB) of the circuit while the lower bound is determined by its noise floor. In general, noise is any random fluctuation that, when added to a signal, reduces its information content. Therefore, the noise level strongly affects the minimum power of a signal that can be used in the circuit to process information. This eventually has a direct impact on the battery lifetime and cost of modern wireless communication systems. Hence, understanding the noise mechanism of devices and how to design a circuit at its lowest noise level is a crucial and fascinating subject.

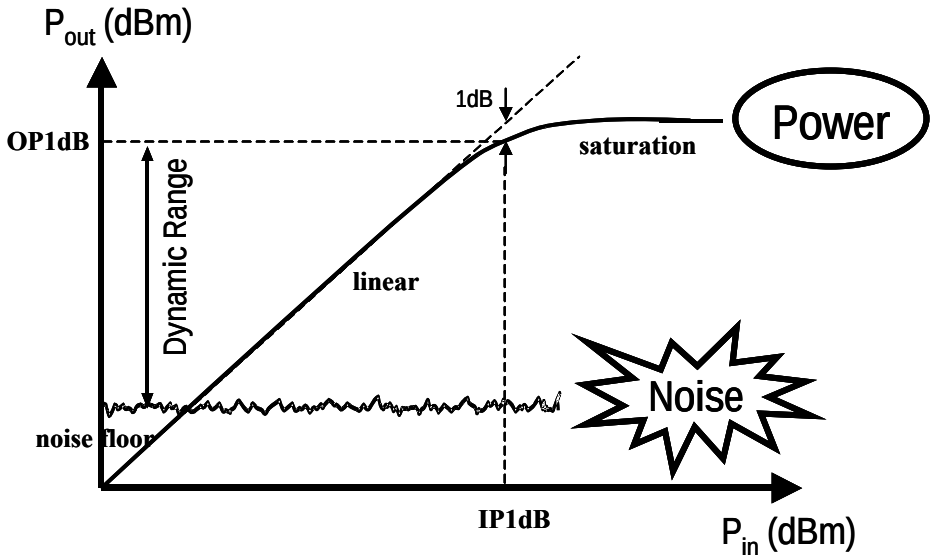


Figure 1.1: Noise floor and dynamic range of an electronic system.

Noise can be passed into a circuit from external noise sources as well as generated within the circuit itself. In an electronic system, intrinsic noise is usually generated by random motions of charge carriers in materials and devices. Such motions can be caused by several mechanisms leading to several noise sources. To name just a few:

- Thermal noise or Johnson noise is caused by thermal motion of charge carriers under equilibrium conditions.
- Shot noise describes the random fluctuations in a signal due to the random arrival time of the charge carriers.
- Flicker noise results from the impurities in a conducting channel which causes fluctuation not only in the number of charge carriers in the channel, but also in their mobility.

Since noise is random in nature, it can be represented by a time-varying random variable *X(t)* with mean value $\overline{X}$, variance $\overline{X^2}$ and power spectral density (PSD) S*(f)*. By definition, S*(f)* represents the time-averaged noise power over a 1 Hz bandwidth at any given frequency *f*. It is an important characteristic of a random signal because it describes how the noise power is distributed in the frequency domain. Thermal noise generated by the resistor and shot noise generated at the p-n junction both have constant PSDs for all frequencies. They are also called white noise. While flicker noise has its PSD proportional to *1/f,* and at low frequency, it is a dominant source of noise.

1.2 Challenges in High Field Noise Modeling for Nanometer MOSFETs

Aggressive scaling technology beyond 100 nm has been greatly improving the RF performance of MOSFETs with cut-off frequency f_T above 460 GHz and minimum noise figure

NF_{MIN} less than 1 dB in the 10 GHz range [1]. Such impressive performance makes low cost CMOS technology a strong candidate for RF and mixed signal integrated circuit applications, even comparable to the state-of-the-art GaAs-pHEMT [2] in terms of noise.

So far there has been considerable work in explaining the noise mechanism of MOSFET devices. Van der Ziel [3]-[4] was the first to analyze the noise behavior of JFETs, followed by Shoji [5]; later Klaassen [6] successfully extended the results to MOSFETs. However, as MOSFETs were scaled down into the sub-micron region, Jindal [7] observed a significant increase in the channel thermal noise predicted by these pioneering works for devices with gate length below 1 μm working in saturation conditions. The excess thermal noise mechanism in scaled MOSFETs has generated intense research [8]–[14] over the years. Some approaches [8]-[10] considered channel noise to have a thermal origin, and the excess noise to be due to the hot-carrier effect. As a short-channel MOSFET goes into saturation, the drain side of the device is under very high electric field, which makes the thermal noise assumption in this region inappropriate. Using a totally different argument, Chen and Deen [11] believe that the noise contribution of the high field drain region is negligible since carriers in the region travel at their saturation velocity, and they do not respond to the electric field fluctuation caused by any noise mechanism if it exists. Chen and Deen [11] then attribute the excess thermal noise to the channel length modulation effect as well as the hot-carrier effect in the low field source region. The argument has been the basis for other works [12]–[13] that focused on modeling the low field source side of MOS devices. However, Scholten et al. [14] have recently reported that the source-side thermal noise model can underestimate the measured noise data of a 100 nm gate length MOSFET device. The results clearly call into question whether the noise contribution of the high field drain region should be ignored.

Considering a device with 100 nm gate length under source-drain bias voltage of 1 V, the average field across the channel far exceeds the saturation field in silicon. In this case, the high field drain region of the device occupies a large portion of the channel, which should strongly affect the device characteristic including its noise behavior. Furthermore, according to Shockley et al. [15], the general noise sources in semiconductor devices are described by

$$\overline{j_n^2(x)} = 4q^2 Dn\Delta f \tag{1.1}$$

where $j_n(x)$ is the volume density for the spectral density of the noise current at x, D is the field dependent diffusion constant of the carriers, and n is the carrier density. Although carriers in the high field saturation region may not directly respond to fluctuation of the high field, they may collide with the lattice, which finally results in their random movements with spherical distributions. If we assume uniform carrier density in the cross-sectional area A of the device, then (1.1) obviously describes a displacement noise current $i_n(x) = j_n(x)A$ produced by random motion of carriers in the high field saturation region within the distance Δx.

Therefore, modeling high frequency noise for nanometer MOSFETs under high field effects will continue to provide challenges as the device process is scaled down further to 45 nm or 30 nm technology nodes.

1.3 Organization of Work

The goal of this research is to develop a framework to fulfill the challenge of high frequency noise characterization and modeling of nanometer MOSFETs under high field. The research work is organized as follows:

Chapter 2 details the high frequency noise characterization of 120 nm CMOS technology. A new procedure of noise source extraction is developed from the measured noise parameters and scattering parameters (S-parameters).

Chapter 3 presents a new analytical noise formulation for nanometer MOSFET devices working in saturation. A channel thermal noise model of the source side, including field-dependent mobility and carrier temperature, is derived. Then, the high field noise in the drain region is developed based on Statz's noise theory for GaAs MESFETs [16] which successfully interpreted (1.1) using an unrelaxable drifting-dipole concept. In addition, based on the two-section channel noise model, the induced gate noise model is derived along with its correlation to the channel noise. The model has been extensively verified and has shown excellent agreement with measured data for 120 nm MOSFET technology. Finally, the model is incorporated into circuit simulators like Spectre or ADS to improve the noise parameter prediction of foundry-provided compact models.

Chapters 4 and 5 discuss the design and implementation of fully integrated low noise amplifiers (LNA) using 120 nm CMOS technology. In general, the most critical step in LNA designs, especially for wideband applications, is to simultaneously match noise and source impedance. This can be achieved by new proposed designs described in these chapters based on the Smith chart. Experimental results are reported and compared with the other published works to validate the design methodologies. The designed LNAs also serve to validate the proposed high-field noise model for nanometer MOSFETs at the integrated circuit level.

Finally, a summary will be presented and a discussion of future extensions to the work completed here will be provided in Chapter 6.

2. HIGH FREQUENCY NOISE MEASUREMENTS

2.1 High Frequency Noise Sources in MOSFETs

High frequency noise of MOSFETs results from both intrinsic and extrinsic noise sources. The extrinsic noise sources are the Johnson noise generated by parasitic components such as the drain/source terminal resistances R_D-R_S, gate electrode resistance R_G, and bulk resistance R_B. The intrinsic noise sources come from the fluctuations of charges within the MOSFET channel. These fluctuations will propagate to the drain and gate terminals to form drain noise (i_d) and induced gate noise (i_g), which have the noise spectral densities of S_{id} and S_{ig}, respectively. Figure 2.1 describes the typical cross-section of a MOSFET as well as its equivalent small-signal model with two noise sources i_d and i_g. Detailed discussion of the

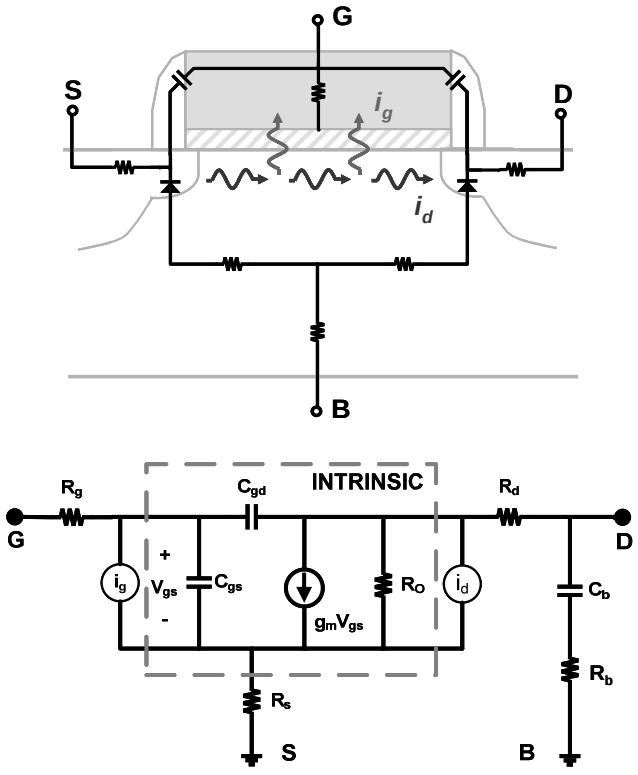


Figure 2.1: Cross-sectional MOSFET description and its equivalent small-signal model with two noise sources: drain noise i_d and induced gate noise i_g.

intrinsic noise sources of MOSFETs and their physical models to describe high-field effects as the gate length entering the nanoscale region will be presented in Chapter 3.

2.2 High Frequency Noise Measurement of MOSFETs

2.2.1 Noise parameters of two-port networks

The noise sources in MOSFETs cannot be measured directly, but must be extracted from experimental noise parameters, which are described by the minimum noise figure NF_{MIN}, the equivalent noise resistance R_N, and the optimum source admittance Y_{OPT}. To determine device noise parameters requires the measurement of noise factor F or noise figure NF, both of which are originally defined by Friis [17]:

$$F = \frac{S_{in} / N_{in}}{S_{out} / N_{out}} \tag{2.1a}$$

$$NF = 10\log_{10} F \ \text{(dB)} \tag{2.1b}$$

The noise figure NF represents the degradation in the signal-to-noise ratio (SNR) as the signal passes through the linear two-port network. NF not only depends on the noise characteristic of the network but also is a function of the source admittance $Y_S = G_S + jB_S$ (Figure 2.2), and the relation is expressed by the well-known expression

$$F = F_{MIN} + \frac{R_N}{G_S}\left|Y_S - Y_{OPT}\right|^2 \tag{2.2}$$

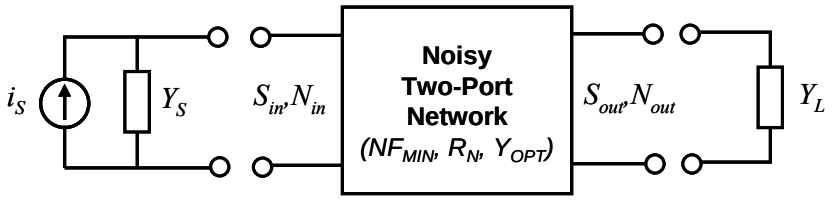


Figure 2.2: Model of a noisy two-port network.

In (2.2), the noise factor F of a linear two-port system exhibits a 3D-parabolic dependence on the source admittance at a single frequency as shown in Figure 2.3. When the source admittance Y_S is tuned to the optimum value Y_{OPT}, the noise factor F of the device reaches its minimum value F_{MIN}. Meanwhile, the equivalent noise resistance R_N represents the sensitivity of the noise factor to the changes in source admittance.

If G and N_a are the power gain and the added noise power from the two-port network, respectively, then the total noise power at the output of the network is given by

$$N_{out} = N_a + GN_{in} \tag{2.3}$$

The noise powers may also be described in terms of the effective noise temperatures such that $N_{in} = kT_sB_n$, where B_n is mainly determined by the equivalent noise bandwidth of the receiver in the noise figure meter (typically 4 MHz), and (2.3) becomes

$$N_{out} = N_a + kGBT_s \tag{2.4}$$

Clearly from (2.4), for the source temperature T_s at absolute zero, the output noise power

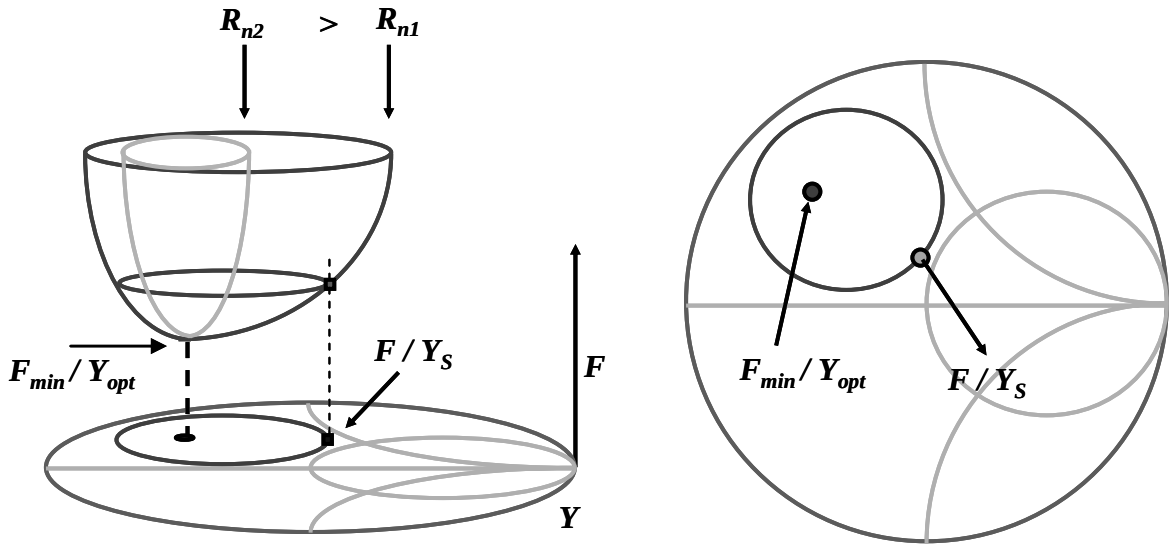


Figure 2.3: Noise parameters of a linear two-port network and its dependence on the source admittances at a single frequency.

measured by the noise figure meter is the noise added by the two-port network. In practice, only two states, "hot" (T_H) and "cold" (T_C), of the noise source are enough to determine N_a, and hence the noise factor F. Since there is always impedance mismatch between the source and the input of the two-port network, additional information about the S-parameters of the network must also be known to determine the available gain, and thus the actual output noise power N_{out}. If the noise factor of the two-port network can be measured for at least four source admittances Y_S, then the noise parameters (F_{MIN}, R_N, Y_{OPT}) can be determined as indicated by (2.2). If measurements are taken for more than four source admittances using the tuner, a least-square technique introduced by Lane [18] can be used to determine the noise parameters of the two-port network. In this way, the results are less susceptible to errors which may occur if two or more source admittances are redundant. The described approach is also known as the Y-factor method [19].

In the Y-factor method, the assumption of equal source admittances for both "hot" and "cold" states can cause errors in noise figure measurements [20]. To overcome the problem, Adamian and Uhlir [21] were the first to introduce the "cold source" technique to measure the noise parameters of a two-port network. In the calibration process, only one measurement of hot and cold output noise powers generated by the noise source is necessary. Then at least three other "cold" output noise powers generated by passive one-port terminations for different source admittances are required to fully characterize the kGB factor of the noise receiver. In the measurement step, there is no involvement of the noise source. Only cold output noise powers of the two-port network cascaded with the noise receiver as a function of source admittance are measured. Next, the noise parameters of the completed system can be determined from the knowledge of the source admittance, the S-parameters of the linear two-port as well as the input

reflection coefficient of the noise receiver. Finally, noise parameters of the linear two-port are obtained by using the correlation matrix method [22] to de-embed them from the overall measured noise parameters of the system. This approach significantly improves the accuracy of the measured noise parameters compared to the Y-factor method since there is only one measurement involving altered temperature states of the noise source. Even in the case where there may be changes in source admittance at different temperature states, they can also be accounted for as described in the practical implementation of this noise measurement technique [23].

2.2.2 Noise-parameter measurements

The noise parameters of active devices are measured from 2 to 26 GHz using the ATN−NP5B automated noise figure measurement system with equipment configuration shown in Figure 2.4. The system is developed based on the "cold source" technique proposed by Adamian and Uhlir [21] as described in the previous section. It consists of a mismatched noise source (MNS), a remote receiver module (RRM), and a mainframe controller unit. The switching circuitry inside the MNS and RRM enable the system to do calibrations and measurements without mechanically breaking connections. The device noise figure is measured for various source admittances, and the noise parameters are extracted using a least-square fit algorithm. Together with the HP 4142 SMU and Agilent 8364A PNA, the system is also capable of doing full DC (I-V curves) and RF (S-parameters) characterizations.

Testing structures have been developed and measured to study the high-field noise behaviors of MOSFETs as their gate lengths are aggressively scaled down into the nanometer regime. The devices under test (DUTs) in this study are n-MOSFETs using 120 nm CMOS

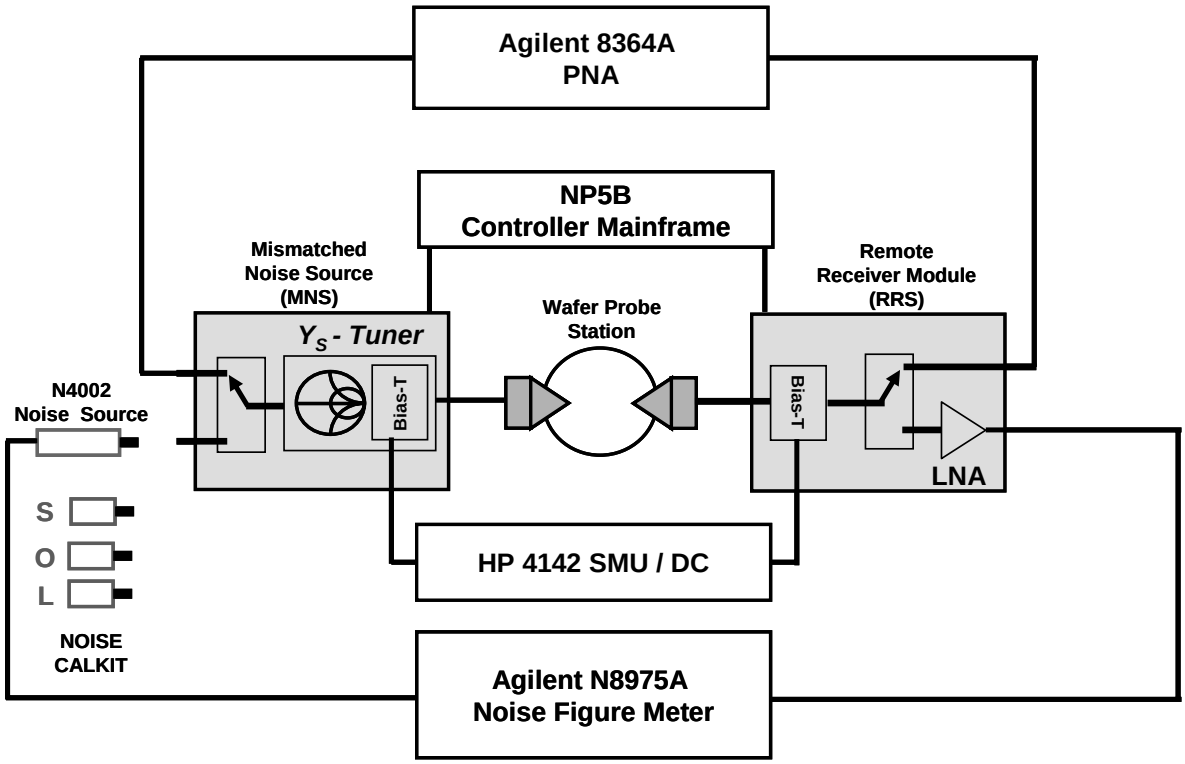


Figure 2.4: Setup of the ATN-NP5B automated noise figure measurement system.

technology. The complete list of the DUTs is given in Table 2.1. Figure 2.5 shows the measured associated gain G_A and the noise parameters of FET2 and FET3 including probe pads. Note that the optimum source admittance Y_{OPT} (or impedance Z_{OPT}) is a complex number and can be expressed in terms of optimum source reflection coefficients Γ_{OPT}, as seen by

$$\Gamma_{OPT} = \frac{Y_0 - Y_{OPT}}{Y_0 + Y_{OPT}} = \frac{Z_{OPT} - Z_0}{Z_{OPT} + Z_0} \tag{2.5}$$

where $Z_0 = 1/Y_0$ is the impedance of the measurement system (typically 50 Ω).

Table 2.1 List of n-MOSFETs for high-field noise study

DUT	Dimensions					Description
	L (nm)	Wf (um)	Nf	M	Total Width	
FET1	240	7.2	16	1	115.2	Length Scaling Effects
FET2	180	7.2	16	1	115.2	
FET3	120	7.2	16	1	115.2	
FET4	120	6.3	16	2	201.6	Width Scaling Effects
FET5	120	4.8	16	2	153.6	
FET6	120	3.6	16	2	115.2	

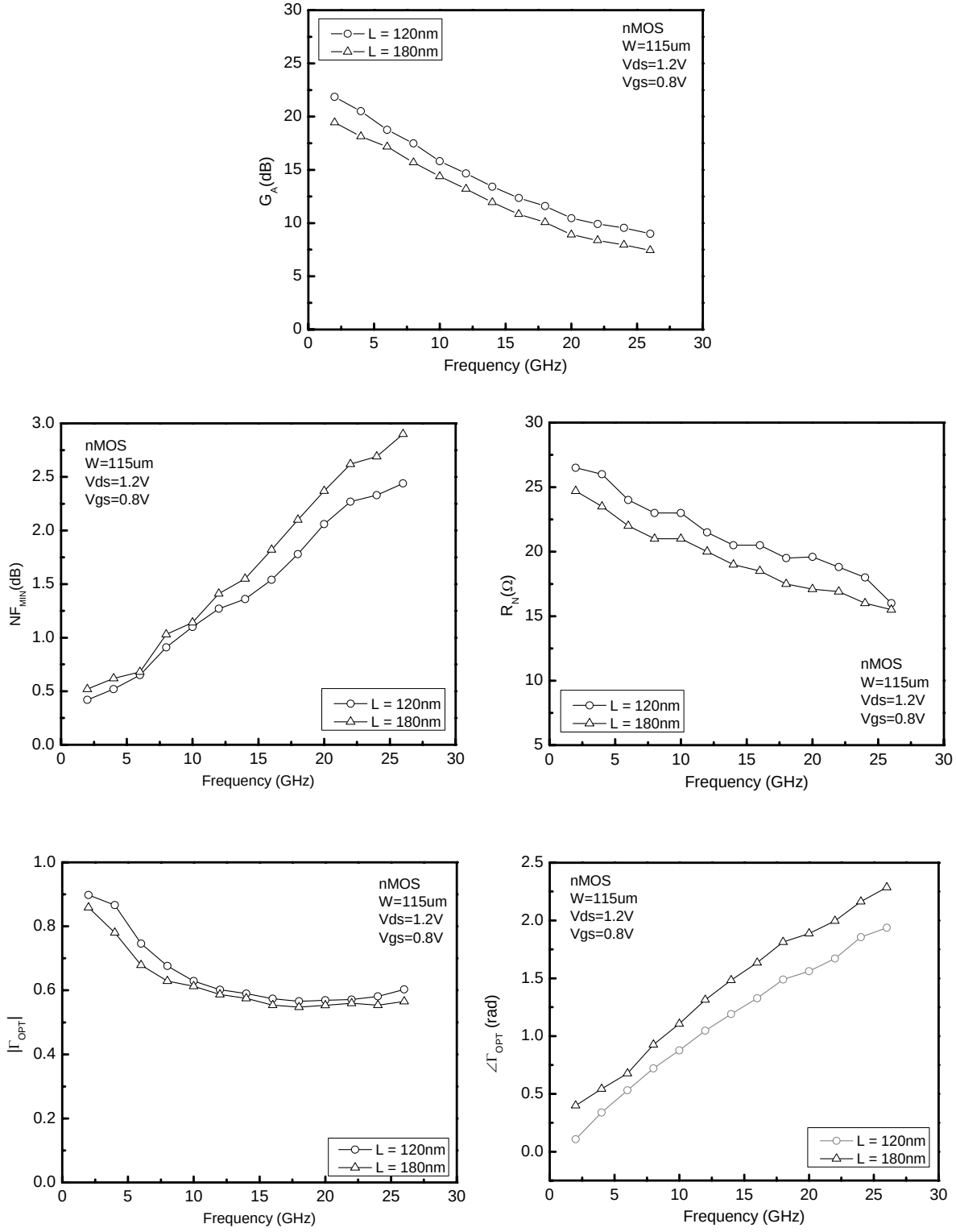


Figure 2.5: Measured associated gain G_A and noise parameters (NF_{MIN}, R_N and Γ_{OPT}) of n-MOSFETs with channel lengths of L = 120 nm and L = 180 nm, respectively.

As observed in Figure 2.5, when the device gate length is scaled down, the gain is increased but the minimum noise figure NF_{MIN} is decreased. This fact confirms the advantage of scaling technology. Also, since R_N is increased as gate length is scaled down, the noise behaviors of small devices are more sensitive to any variation of source impedance, and hence it is more difficult to design input noise matching networks.

2.3 Extractions of High Frequency Noise Sources in MOSFETs

Figure 2.6(a) shows a typical layout of an n-MOSFET (L = 120 nm, W = 115 um) with RF pads. Dummy structures of "Open" and "Short" (Figure 2.6 (b), (c)) are used to bring the measurement planes to the actual DUT reference planes [24]. From the measured high frequency (HF) noise parameters and S-parameters of the DUTs as well as the measured S-parameters of those dummy structures, intrinsic noise sources S_{id}, S_{ig} and their cross-correlation

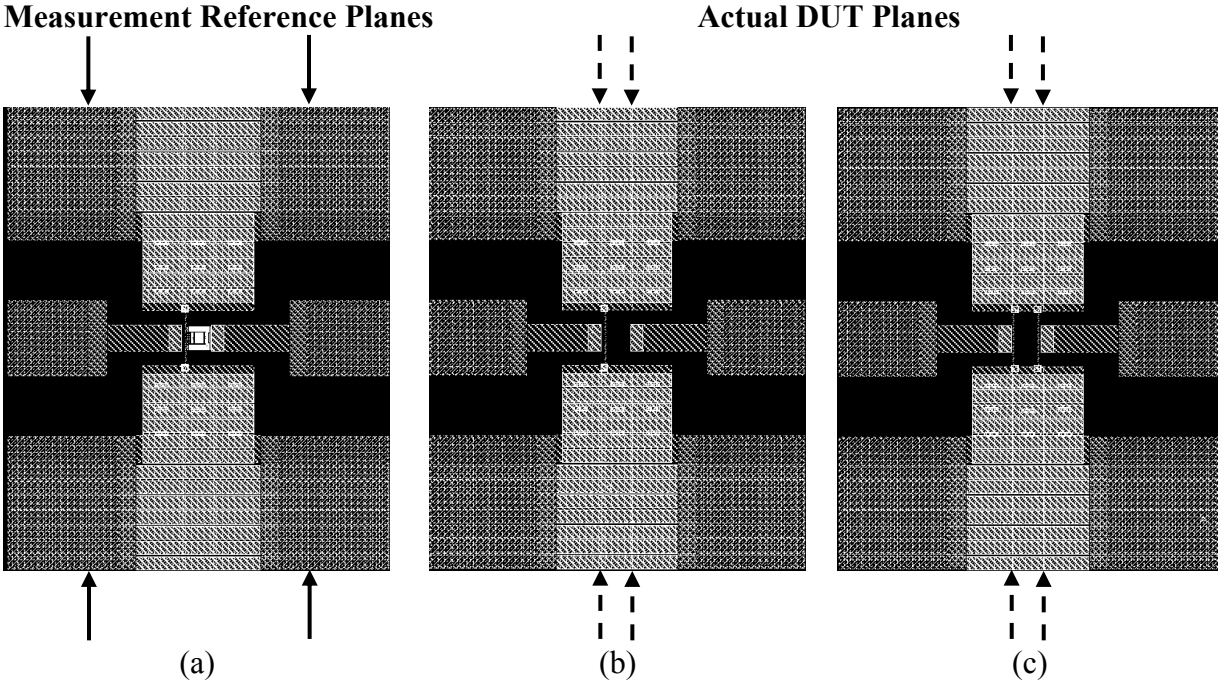


Figure 2.6: (a) Layout of an n-MOSFET (L = 120 nm, W = 115 μm) with RF pads and off-wafer calibration reference planes. (b) "Open" standards. (c) "Short" standards.

S_{ig-id} can be directly extracted. At the University of Illinois, a new noise source extraction procedure is developed, which includes three main steps (i) to remove the effects of probing pads, (ii) to further de-embed the measured data (both noise and S-parameters) from extrinsic to intrinsic level using Engberg's approach [25] to exclude the contribution of device parasitics such as drain/source terminal resistances R_D-R_S, gate electrode resistance R_G, and bulk resistance R_B, and (iii) to calculate the power spectral densities of the noise sources and their correlation. This approach is much simpler and more efficient than the proposed method in [26]. Detail steps involving the de-embedding procedure are described in Figure 2.7.

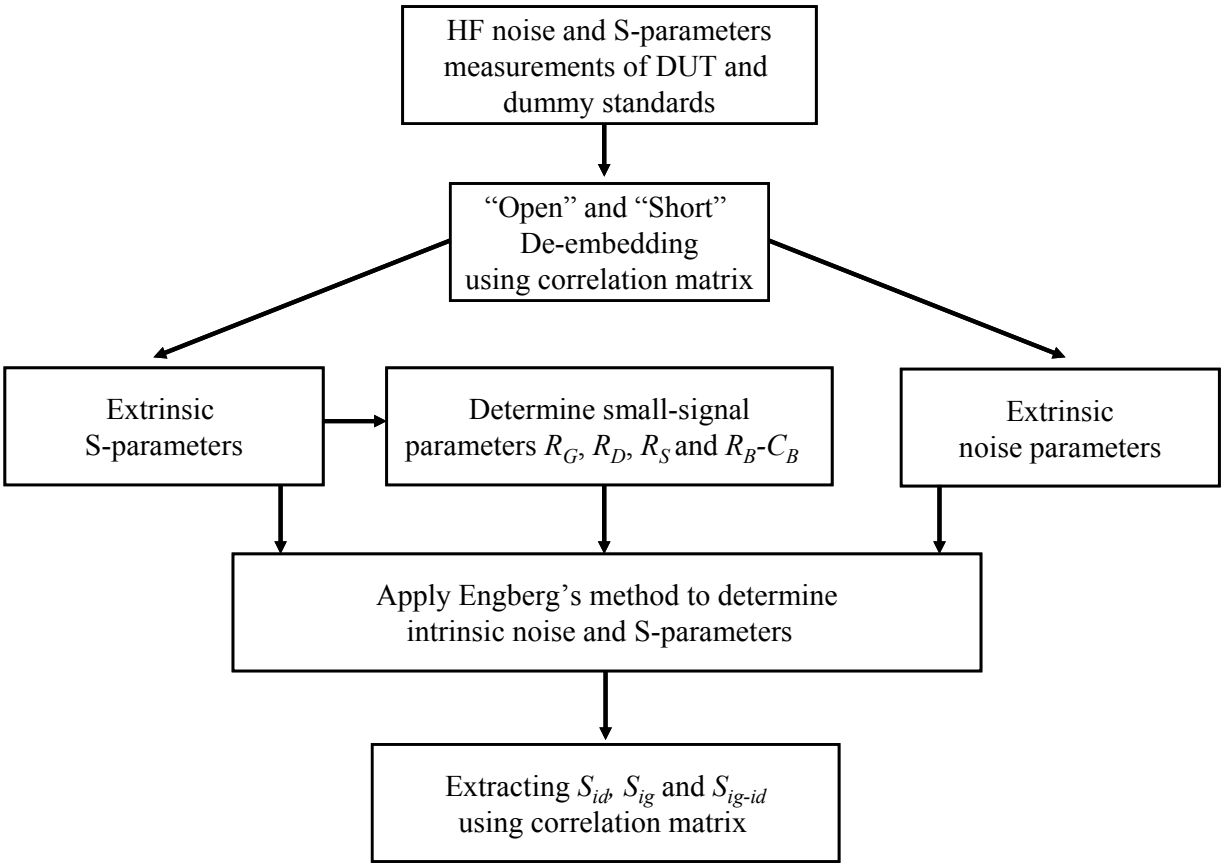
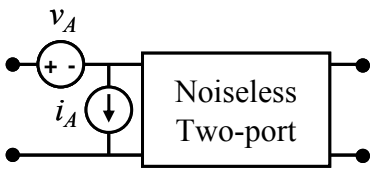
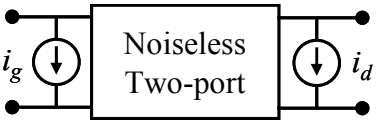


Figure 2.7: Flow chart of noise source extraction procedure.

In linear noise analysis [22], the chain correlation matrix C_A of any two-port network can be described by its noise parameters. However, as shown in Figure 2.1, the equivalent noise circuit of a MOSFET is in the admittance form which is represented by correlation matrix C_Y. Therefore, the transformation of C_A to C_Y as summarized in Table 2.2 is necessary to determine the noise current sources in MOSFET.

Table 2.2 Correlation-matrix transformation of a linear two-port network

Representation	Chain	Admittance
Two-port		
Correlation Matrix	$C_A = \frac{1}{2}\begin{bmatrix} v_A v_A^* & v_A i_A^* \\ v_A^* i_A & i_A i_A^* \end{bmatrix}$	$C_Y = \frac{1}{2}\begin{bmatrix} i_g i_g^* & i_d i_g^* \\ i_d^* i_g & i_d i_d^* \end{bmatrix}$
Noise parameters and correlation matrix	$C_A = 2kTR_N \begin{bmatrix} 1 & \frac{NF_{MIN}-1}{2R_N} - Y_{OPT} \\ \frac{NF_{MIN}-1}{2R_N} - Y_{OPT}^* & \lvert Y_{OPT} \rvert^2 \end{bmatrix}$	$C_Y = TC_A T^\dagger$
Transformation matrix	[S] → [Y] → $T = \begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}$	

From the measured intrinsic noise and S- (or Y-) parameters, the power spectral densities of drain noise S_{id}, induced gate noise S_{ig}, and their correlation $S_{ig\text{-}id}$ of the DUT are determined, as seen by

$$S_{id} = \overline{i_d i_d^*} = 4kTR_N \left| Y_{21} \right|^2 \tag{2.6}$$

$$S_{ig} = \overline{i_g i_g^*} = 4kTR_N \left\{ \left|Y_{11}\right|^2 + \left|Y_{OPT}\right|^2 - 2\,\mathrm{Re}\left[Y_{11} \left(\frac{F_{MIN} - 1}{2R_N} - Y_{OPT} \right) \right] \right\} \tag{2.7}$$

$$S_{ig-id} = \overline{i_g i_d^*} = 4kTR_N \left[Y_{11} - \left(\frac{F_{MIN} - 1}{2R_N} - Y_{OPT} \right) \right] Y_{21}^* \tag{2.8}$$

where k = 1.38×10^{-23}J/K is the Boltzmann constant. Figure 2.8 shows the noise source extraction results for an n-MOSFET with L = 120 nm and W = 115 μm from the 2−26 GHz noise and S-parameters measured data. The drain noise is approximately independent of frequency while the induced gate noise is proportional to f^2 as expected. The cross-correlation of the two noise sources is mainly imaginary, which explains the coupling effects through gate oxide capacitor C_{OX}.

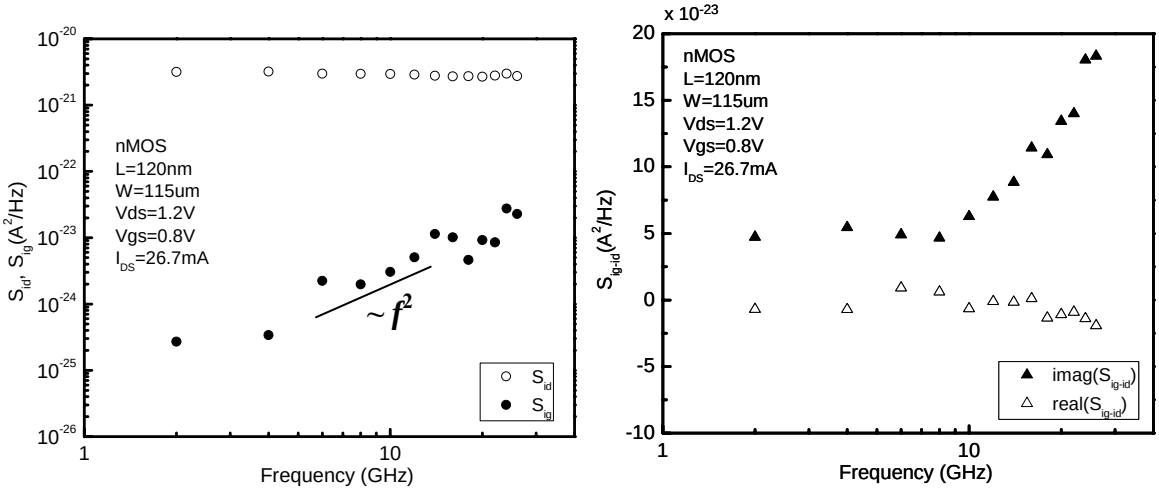


Figure 2.8: Extracted drain noise S_{id}, induced gate noise S_{ig} and cross-correlation $S_{ig\text{-}id}$ for an n-MOSFET with L = 120 nm, W = 115 μm biased at V_{DS} = 1.2 V and V_{GS} = 0.8 V.

3. DRIFTING-DIPOLE NOISE (DDN) MODEL FOR NANOMETER MOSFETS

3.1 Drain Noise Modeling

3.1.1 MOSFET channel under high lateral field effect

Figure 3.1 shows a typical cross-section of a nanometer MOSFET structure. Within the effective gate length L_{EFF}, we assume a piece-wise approximation of carrier drift velocity v [27]

$$v = \begin{cases} \mu_{EFF} E / \left(1 + E / E_C\right), & (E < E_C) \\ v_{SAT}, & (E > E_C) \end{cases} \tag{3.1}$$

where v_{SAT} is the carrier saturation velocity, μ_{EFF} is the effective mobility, E is the lateral quasi-Fermi electric field, and $E_C = 2v_{SAT}/\mu_{EFF}$ is the critical or saturation field. When the maximum lateral electric field in the channel exceeds the value of E_C at the critical point, the channel of the MOSFET is divided into two regions: Region I of low field ohmic property and Region II of high field saturation velocity. The critical point is going to shift to the source side if the drain voltage continues to increase.

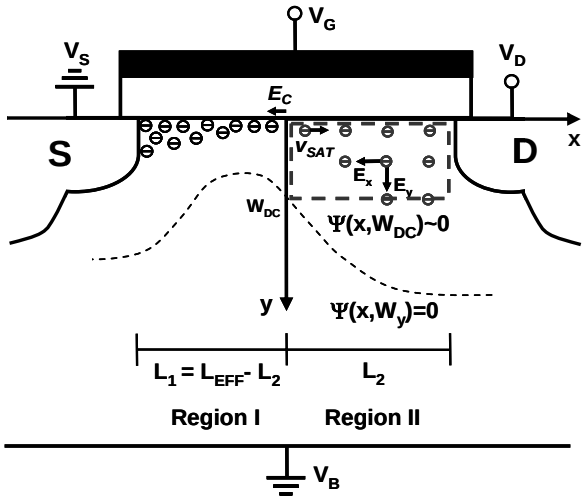


Figure 3.1: Cross-sectional MOSFET description: (I) low field ohmic property, (II) high field saturation velocity.

In Region I, we employ the gradual channel approximation (GCA) and consider the effective mobility μ_{EFF} as a function of both gate voltage V_{GS} and drain voltage V_{DS} [28]-[30],

$$\mu_{EFF} = \frac{\mu_0}{1+\theta\left(V_{GS}-V_T\right)+\gamma V_{DS}} \tag{3.2}$$

where μ_0 is the low field mobility, $\theta = \theta_0 / t_{OX}$ is the surface scattering factor, $\gamma = (\gamma_0\mu_0)/(2v_{SAT}L_{EFF})$ is the lateral mobility reduction factor, θ_0 and γ_0 are empirical parameters, and V_T is the threshold voltage.

In Region II, the GCA fails because the vertical field no longer dominates the lateral field. As a result, the potential distribution Ψ in the space charge region becomes two-dimensional and is the solution of Poisson's equation,

$$\nabla^2\Psi\left(x,y\right) = \frac{qN_A}{\varepsilon_{Si}} \tag{3.3}$$

Equation (3.3) assumes carrier accumulation is negligible due to high applied voltage at the drain side, and N_A is the average doping density in the substrate. A particular solution of (3.3) is also the potential in Region I to guarantee the continuity of potential at the boundary between the two regions, and is given by the parabolic relation everywhere in the carrier stream [31]:

$$\Psi^P\left(x,y\right) = \Psi_S\left(1-\frac{y}{W_{DC}}\right)^2 \tag{3.4a}$$

$$\Psi_S = V_C + 2\Psi_F + \frac{2kT_0}{q}\ln\left[\frac{C_{OX}\left(V_{GS}-V_{FB}-2\Psi_F\right)}{\sqrt{2\varepsilon_{Si}kT_0N_A}}\right] \tag{3.4b}$$

$$W_{DC} = \sqrt{\frac{2\varepsilon_{Si}\Psi_S}{qN_A}} \tag{3.4c}$$

$$V_C = \frac{V_{GT}E_CL_1}{V_{GT}+aE_{SAT}L_1} \tag{3.4d}$$

where Ψ_S is the surface potential, V_C is the quasi-Fermi potential at the critical point [27], Ψ_F is the separation of the Fermi potential from the middle of the bandgap, V_{FB} is the flatband voltage, a is the coefficient accounting for the body effect on the threshold voltage, W_{DC} is the depletion depth at the critical point, L_1 is the length of Region I, C_{OX} is the gate capacitance per unit area, k is the Boltzmann constant, T_0 is the ambient temperature, and $V_{GT} = V_{GS} - V_T$. In addition to the particular solution, we have to add the homogeneous or Laplace solution to satisfy the boundary conditions,

$$\Psi^L(0, y) = 0 \tag{3.5a}$$

$$\Psi^L(x, W_{DC}) = 0 \tag{3.5b}$$

$$E_x^L(0,0) = \frac{\partial \Psi^L(0,0)}{\partial x} = E_C \tag{3.5c}$$

In (3.5b), we assume most of the carriers in Region II concentrate within the depletion depth of W_{DC}. Following Grebene's approach [32], and approximating the solution to the lowest space harmonic, we obtain

$$\Psi^L(x, y) = \frac{2E_C W_{DC}}{\pi} \sinh\left(\frac{\pi x}{2W_{DC}}\right) \cos\left(\frac{\pi y}{2W_{DC}}\right) \tag{3.6}$$

From (2.4) and (2.6), the source-drain potential V_{DS} is evaluated at $x = L_2$ and $y = 0$, as seen by

$$V_{DS} = -\Psi_{bi} + V_C + 2\Psi_F + V_H + \frac{2E_C W_{DC}}{\pi} \sinh\left(\frac{\pi L_2}{2W_{DC}}\right) \tag{3.7}$$

where Ψ_{bi} is the built-in potential of the drain-to-substrate junction, V_H is accounted for surface potential at strong inversion in (3.4b), and is given by

$$V_H = \frac{2kT_0}{q} \ln\left[\frac{C_{OX}\left(V_{GS} - V_{FB} - 2\Psi_F\right)}{\sqrt{2\varepsilon_{Si} kT \overline{N_A}}}\right] \tag{3.8}$$

Since $L_{EFF} = L_1 + L_2$, (3.7) is clearly an implicit equation of the unknown L_2 which can be solved numerically.

For the sake of simplicity, in this work, we have considered the average effect in modeling the carrier transport in a nanometer MOSFET, although under high applied E-field some other non-equilibrium phenomena can happen, e.g., velocity overshoot [33]-[34]. Nonetheless, recent reports [35]-[36] have confirmed that carrier velocity at the source side still depends strongly on the mobility μ_{EFF}, and average carrier velocity at room temperature is not yet in the overshoot regime even for sub-100 nm devices, thus justifying our approximation.

3.1.2 Channel noise generated by fluctuations in low field region

In this section we evaluate the open-circuit noise voltage at the drain due to voltage fluctuation ΔV_1 of an infinitesimal segment within the channel of Region I. First of all, under the applied E-field, carriers in the region gain energy and their effective temperature T may increase above the ambient temperature T_0 following the relation [37]

$$T(x) = T_0\left[1+\delta\left(\frac{E}{E_C}\right)^2\right] \tag{3.9}$$

where the hot electron temperature coefficient δ is an empirical parameter. When the device is under strong inversion, the current I_D is dominated by drift current. Using piece-wise approximation of the carrier velocity as described by (3.1), we can derive the I-V relation in Region I of the channel [27], as seen by

$$I_D = \mu_{EFF} W_{EFF} C_{OX}\left(V_{GT} - aV\right)\frac{E}{1+\left(E/E_C\right)} \tag{3.10}$$

At the end of Region I where $E = E_C$ and $V = V_C$, we obtain

$$I_D = \mu_{EFF} W_{EFF} C_{OX} \left(V_{GT} - aV_C \right) \frac{E_C}{2} \tag{3.11}$$

Because the current in the channel is continuous, from (3.10) and (3.11) we can calculate the ratio E/E_C and re-express (3.9) as a function of the quasi-Fermi potential:

$$T(x) = T_0 \left[1 + \delta \left(\frac{V_{GT} - aV_C}{V_{GT} + aV_C - 2aV} \right)^2 \right] \tag{3.12}$$

Although carriers in the channel become "hot" as the applied field increases, the average velocity of the carriers is still smaller than their thermal velocity. Hence, the equilibrium condition still holds, and the voltage fluctuation ΔV_1 can be modeled by thermal noise with mean square value,

$$\frac{\overline{\Delta V_1^2}}{\Delta f} = 4kT\Delta R = 4kT \frac{\Delta V}{I_D} \tag{3.13}$$

where ΔV is the voltage drop across the resistance ΔR of the infinitesimal segment in Region I.

In Appendix A, we give the derivation of the noise fluctuation at the drain terminal ΔV_{D1} as a consequence of the thermal noise ΔV_1 generated in Region I. The result is

$$\Delta V_{D1} = M \left(\frac{V_{GT} - aV}{V_{GT} - aV_C} \right) \Delta V_1 \tag{3.14}$$

Substituting (3.12) and (3.14) into (3.13), we obtain the mean square value of the drain noise voltage ΔV_{D1} caused by the infinitesimal voltage fluctuation ΔV_1 in Region I,

$$\frac{\overline{\Delta V_{D1}^2}}{\Delta f} = \frac{4kT_0 M^2}{I_D} \left[\left(\frac{V_{GT} - aV}{V_{GT} - aV_C} \right)^2 + \delta \left(\frac{V_{GT} - aV}{V_{GT} + aV_C - 2aV} \right)^2 \right] \Delta V \tag{3.15}$$

At the drain terminal, the total contribution of all noise sources along the channel in Region I is therefore a straight integration of (3.15) between the limits of $V = 0$ and $V = V_C$.

The final result is

$$\frac{\overline{V_{D1}^2}}{\Delta f} = \frac{4kT_0M^2}{I_D}\left\{\frac{a^2V_C^3 - 3aV_{GT}V_C^2 + 3V_{GT}^2V_C}{3\left(V_{GT} - aV_C\right)^2}\right.$$

$$\left. + \frac{\delta(V_{GT} - aV_C)}{4a}\left[\left(\frac{2aV_{GT}V_C}{V_{GT}^2 - a^2V_C^2}\right) + \ln\left(\frac{V_{GT} + aV_C}{V_{GT} - aV_C}\right)\right]\right\} \quad (3.16)$$

The drain noise model in (3.16) represents the "enhancement" of thermal noise contributed by carriers in Region I through the "hot carrier" effect and the hyperbolic factor *M*, which accounts for the noise-induced channel length modulation.

3.1.3 Channel noise generated by drifting dipoles in high field region

Under strong applied E-field at the drain side, Region II is clearly in a non-equilibrium condition. As stated earlier by (1.1), there should be a displacement noise current $i_n(x)$ associated with carriers drifting at v_{SAT} due to their own rapid random motion. At any position x within the spatial interval Δx, the noise current $i_n(x)$ consists of short impulses, uncorrelated from one instant of time to the next. Comparing (1.1) to the shot noise expression, $i_n(x) = 2qI$ at rate $r = I/q$, the sequence of current impulses is clearly generated at the rate

$$r = \frac{2DnA}{\Delta x} \quad (3.17)$$

In addition, each of the current impulses displaces a charge q across the interval Δx, thus resulting in an electric dipole layer of charge density $\sigma = q/A$ at x_0 and $-\sigma$ at $x_0 + \Delta x_0$. Since the carriers in the saturation velocity region do not respond to the applied E-field, the resulting dipole layers are unable to recover and drift unchanged to the drain terminal. In this section, for the first time we apply Statz's analytical treatment of high field noise [16] to

calculate the perturbation effect of the dipole potential difference on a MOSFET drain terminal under open-circuit conditions. As shown in Appendix B, the dipole potential difference at position $x = x_0$ can be approximated by

$$\Psi_{DP}(x,y) = \pm\left(\frac{2\sigma}{\pi\varepsilon_{Si}}\right)\cos\left(\frac{\pi y}{2W_{DC}}\right)\exp\left[-\left(\frac{\pi|x-x_0|}{2W_{DC}}\right)\right]\Delta x_0 \tag{3.18}$$

where the (+) sign applies for $x < x_0$ and the (–) sign applies for $x > x_0$. Because the particular potential $\Psi^P(x,y)$ is consistent across the device channel length, $\Psi_{DP}(x,y)$ only has an impact on the Laplace potential $\Psi^L(x,y)$.

For $x < x_0$, to maintain the boundary condition (3.5a), potentials due to charges at the drain will be induced along the channel to cancel the effect of $\Psi_{DP}(x,y)$. At the critical point, the induced potential is seen by

$$\Psi_I(0,0) = -\Psi_{DP}(0,0) = -\left(\frac{2\sigma}{\pi\varepsilon_{Si}}\right)\exp\left(\frac{\pi x_0}{2W_{DC}}\right)\Delta x_0 \tag{3.19}$$

From (3.19), the potential induced on the drain terminal as a result of the formation of dipole-layer potential difference is therefore

$$\Psi_I(L_2,0) = -\left(\frac{2\sigma}{\pi\varepsilon_{Si}}\right)\exp\left[\frac{\pi(L_2-x_0)}{2W_{DC}}\right]\Delta x_0 \tag{3.20}$$

The dipole generated at position $x = x_0$ and time $t = t_i$ will then drift at a steady speed of $v = v_{SAT}$. The induced potential at the drain in (3.20) now becomes time-dependent, as seen by

$$\Psi_I^{t_i}(L_2,t) = -\left(\frac{2\sigma}{\pi\varepsilon_{Si}}\right)\exp\left\{\frac{\pi\left[(L_2-x_0)-v_{SAT}(t-t_i)\right]}{2W_{DC}}\right\}\Delta x_0 \tag{3.21}$$

where $t_i < t < t_i + (L_2 - x_0) / v_{SAT}$

For $x > x_0$, the dipole layers directly affect the drain voltage. However, their potential

contribution is canceled by the corresponding image dipole layers mirrored at plane $x = L_2$.

Equation (3.21) represents one of the many dipole layers randomly generated at the plane $x = x_0$ at different times t_i. We obtain the spectral density of each of these potential differences by applying a Fourier transform,

$$S(f) = \int_{-\infty}^{+\infty} \Psi_1^{t_i}(L_2, t) \exp(-j2\pi ft) dt = \frac{4\sigma W_{DC}}{\pi^2 \varepsilon_{Si} v_{SAT}} \left\{ 1 - \exp\left[\frac{\pi (L_2 - x_0)}{2W_{DC}} \right] \right\} \Delta x_0 \qquad (3.22)$$

S(f) has a very wide spectrum which exponentially decays toward infinity. However, the operating frequency of a nanometer MOSFET is much smaller than the inverse of the carrier transit time through Region II, $v_{SAT} / L_2 \sim 1$ THz. In (3.22) we only evaluate *S(f)* in the limit of $f \to 0$.

Next, let the random process *Y(t)* be the sum of all independent events occurring at different time t_i; then its spectral density *Y(f)* is calculated using Carson's rule as seen by

$$Y(f) = 2r \left| S(f) \right|^2 \qquad (3.23)$$

where the generation rate r is defined by (3.17). At the drain terminal, the noise voltage due to the generation of dipole layers at position $x = x_0$ has the mean square value obtained from (3.17), (3.22), and (3.23):

$$\frac{\overline{\Delta V_{D2}^2}}{\Delta f} = \frac{64nq^2 DW_{DC}}{\pi^4 \varepsilon_{Si}^2 v_{SAT}^2 W_{EFF}} \left\{ 1 - \exp\left[\frac{\pi (L_2 - x_0)}{2W_{DC}} \right] \right\}^2 \Delta x_0 \qquad (3.24)$$

In (3.24), the carrier stream is assumed to flow through the cross-section $A = W_{EFF} W_{DC}$.

Finally, we calculate the total noise voltage produced by all the dipole layers generated across Region II by integrating (3.24) over $0 < x_0 < L_2$. The result is

$$\frac{\overline{V_{D2}^2}}{\Delta f} = \frac{64qI_D DW_{DC}^2}{\pi^5 \varepsilon_{Si}^2 v_{SAT}^3 W_{EFF}^2 x_{j,EFF}} \left[\left(\frac{\pi L_2}{W_{DC}} \right) + 3 - 4\exp\left(\frac{\pi L_2}{2W_{DC}} \right) + \exp\left(\frac{\pi L_2}{W_{DC}} \right) \right] \qquad (3.25)$$

In (3.25), we assume the channel current I_D in the high field region is expressed by

$$I_D = nqv_{SAT}W_{EFF}x_{j,EFF} \tag{3.26}$$

where $x_{j,EFF}$ is considered the effective junction depth at which most of the carriers are collected by the drain terminal.

Since the noise contributions of Regions I and II are uncorrelated, the total open-circuit noise voltage at the drain is given by

$$\frac{\overline{V_D^2}}{\Delta f} = \frac{\overline{V_{D1}^2}}{\Delta f} + \frac{\overline{V_{D2}^2}}{\Delta f} \tag{3.27}$$

Under short-circuit conditions, the voltage fluctuations are transformed into the drain noise currents, as seen by

$$S_{id} = \frac{\overline{i_D^2}}{\Delta f} = \frac{\overline{V_D^2}}{\Delta f} \times \frac{1}{R_O^2} = S_{id1} + S_{id2} \tag{3.28a}$$

$$S_{id1} = \frac{\overline{i_{D1}^2}}{\Delta f} = \frac{\overline{V_{D1}^2}}{\Delta f} \times \frac{1}{R_O^2} \tag{3.28b}$$

$$S_{id2} = \frac{\overline{i_{D2}^2}}{\Delta f} = \frac{\overline{V_{D2}^2}}{\Delta f} \times \frac{1}{R_O^2} \tag{3.28c}$$

where $R_O = \partial V_{DS} / \partial I_D$ is the output conductance of the device, and V_{DS} is given by (3.7).

3.2 Induced Gate Noise Modeling

3.2.1 Gate noise induced by fluctuations in low field region

In low field Region I, any noise voltage ΔV_1 caused by infinitesimal ohmic segments will produce fluctuation charges on the gate through the oxide capacitor C_{OX} of the device, as expressed by

$$\Delta Q_{11} = -W_{EFF} C_{OX} \int_0^{L_1} \Delta V_1 dx' \tag{3.29}$$

In (3.29), we use x' as a new lateral axis, and $x' = 0$ is the beginning of Region I. Under short-circuit condition at the drain, the noise voltage ΔV_1 also creates a fluctuation Δi_{D1} in the channel current as described by (3.28). In high field Region II, the appearance of the fluctuation current Δi_{D1} requires additional charges to the channel current and, hence, induced charges on the gate with opposite sign, as seen by

$$\Delta Q_{12} = -\Delta i_{D1} t_{II} = -\Delta i_{D1} \left(\frac{L_2}{v_{SAT}} \right) \tag{3.30}$$

where t_{II} is the transit time through Region II. The total induced fluctuation charge on the gate is therefore

$$\Delta Q_1 = -W_{EFF} C_{OX} \int_0^{L_1} \Delta V_1 dx' - \Delta i_{D1} \left(\frac{L_2}{v_{SAT}} \right) \tag{3.31}$$

To calculate the induced gate charge ΔQ_1 in (3.31), we have to determine the distribution of the noise voltage ΔV_1 as a function of the position x' along the channel. In Appendix C, we show that

$$\Delta V_1 = \frac{\left(x' + V / E_C \right) \Delta i_{D1}}{\mu_{EFF} W_{EFF} C_{OX} \left(V_{GT} - aV \right)}, \; 0 < x' < x'_0 \tag{3.32a}$$

$$\Delta V_1 = \frac{\left[\left(x' + V / E_C \right) - \zeta \left(L_1 + V / E_C \right) \right] \Delta i_{D1}}{\mu_{EFF} W_{EFF} C_{OX} \left(V_{GT} - aV \right)}, \; x'_0 < x' < L_1 \tag{3.32b}$$

We have modified Statz's formulation in the derivation of (3.32) to account for the nonlinear relation between the carrier velocity and the applied field, which is more appropriate for nanometer MOSFETs, as described by (3.1).

Inserting (3.32) into (3.31) and using the relation [27]

$$x' + \frac{V}{E_C} = \left(\frac{\mu_{EFF} W_{EFF} C_{OX}}{I_D} \right) \left(V_{GT} - \frac{a}{2} V \right) V \tag{3.33}$$

to carry out the integral from $V = 0$ to $V = V_C$, we obtain

$$\Delta Q_1 = -\frac{\mu_{EFF} W_{EFF}^2 C_{OX}^2 \Delta i_{D1}}{I_D^2} \left[P_0 - P_1 \left(V_x - \frac{1}{2} \ln V_x \right) \right] \tag{3.34}$$

where P_0, P_1, and V_x are defined as

$$P_0 = \left(\frac{-a^2 V_C^3 + 3a V_{GT} V_C^2 + 6 V_{GT}^2 V_C}{24a} \right) + \frac{\left(V_{GT} - a V_C \right)^2 \left[\zeta V_C + E_C \left(\zeta L_1 + a L_2 \right) \right]}{2a}$$

$$+ \frac{V_{GT}^2 \left(V_{GT} - a V_C \right)}{4a^2} \ln \left(\frac{V_{GT} - a V_C}{V_{GT}} \right) \tag{3.35}$$

$$P_1 = \left[\frac{\zeta \left(V_C + E_C L_1 \right) \left(V_{GT} - a V_C \right)^2}{2a} \right] \tag{3.36}$$

$$V_x = \frac{V_{GT} - aV}{V_{GT} - a V_C} \tag{3.37}$$

Then, from (3.15), (3.28) and (3.34), the mean square value of the fluctuation charge on the gate due to an infinitesimal noise voltage ΔV_1 in Region I can be expressed by

$$\overline{\Delta Q_1^2} = \frac{4kT_0 \mu_{EFF}^2 W_{EFF}^4 C_{OX}^4 M^2 \Delta f}{R_O^2 I_D^5} \left[V_x^2 + \delta \left(\frac{V_x}{2V_x - 1} \right)^2 \right] \times \left[P_0 - P_1 \left(V_x - \frac{1}{2} \ln V_x \right) \right]^2 \Delta V \tag{3.38}$$

Integrating (3.38) over V from $V = 0$ to $V = V_C$, we obtain the total gate charge fluctuation,

$$\overline{Q_1^2} = \frac{4kT_0 \mu_{EFF}^2 W_{EFF}^4 C_{OX}^4 M^2 \Delta f}{a R_O^2 I_D^5} \left(V_{GT} - a V_C \right) \times \left[P_G \left(\frac{V_{GT}}{V_{GT} - a V_P} \right) - P_G (1) \right] \tag{3.39}$$

where $P_G(\lambda)$ is given in Appendix D. To simplify the integral calculation, we have assumed second order approximation such that

$$V_x - \frac{1}{2}\ln(V_X) = \frac{1}{4}\left(3 + V_x^2\right) \tag{3.40}$$

Because the charge fluctuations are time-dependent, there will be an induced gate noise current flowing into the gate and its mean square value is given by

$$S_{ig1} = \frac{\overline{i_{G1}^2}}{\Delta f} = \omega^2 \frac{\overline{Q_1^2}}{\Delta f} \tag{3.41}$$

3.2.2 Gate noise induced by drifting dipoles in high field region

Since the accumulation charges in the channel of Region II are negligible, the dipole potential difference $\Psi_{DP}(x,y)$ does not directly induce fluctuation charges. However, under short-circuited drain condition, it will cause the noise current Δi_{D2} to flow through the device channel. Since the noise mechanisms in the two regions are independent, there is no potential jump ΔV_1 in this condition, and ζ in (2.31) should be equal to zero. Then from (2.34), we obtain

$$\Delta Q_2 = -\frac{\mu_{EFF} W_{EFF}^2 C_{OX}^2 \Delta i_{D2}}{I_D^2} P_2 \tag{3.42}$$

where P_2 is given by

$$P_2 = \left(\frac{-a^2 V_C^3 + 3aV_{GT}V_C^2 + 6V_{GT}^2 V_C}{24a}\right) + \frac{\left(V_{GT} - aV_C\right)^2 E_C L_2}{2} + \frac{V_{GT}^2\left(V_{GT} - aV_C\right)}{4a^2}\ln\left(\frac{V_{GT} - aV_C}{V_{GT}}\right) \tag{3.43}$$

The induced gate noise current will be calculated directly from the channel noise current, as seen by

$$\overline{i_{G2}^2} = \omega^2 \overline{Q_2^2} = \frac{\omega^2 \mu_{EFF}^2 W_{EFF}^4 C_{OX}^4 \overline{i_{D2}^2}}{I_D^4} P_2^2 \tag{3.44}$$

Inserting (3.25) into (3.44) and using (3.28), we finally get

$$S_{ig2} = \frac{\overline{i_{G2}^2}}{\Delta f} = \omega^2 \frac{64qD\mu_{EFF}^2 W_{EFF}^2 C_{OX}^4 W_{DC}^2}{\pi^5 \varepsilon_{Si}^2 v_{SAT}^3 x_{j,EFF} R_O^2 I_D^3} P_2^2 \left[\left(\frac{\pi L_2}{W_{DC}} \right) + 3 - 4\exp\left(\frac{\pi L_2}{2W_{DC}} \right) + \exp\left(\frac{\pi L_2}{W_{DC}} \right) \right] \tag{3.45}$$

3.3 Correlation of Drain Noise and Induced Gate Noise Currents

Since the total channel noise i_D and the total induced gate noise i_G have parts generated from the same noise sources in the channel, there must be some correlation between them. However, due to independence of the noise mechanisms in Regions I and II, the pair of noise currents (i_{D1},i_{G2}) and (i_{D2},i_{G1}) are uncorrelated. Then the correlation coefficient C of i_G and i_D can be defined as [16]

$$C = \frac{\overline{i_G i_D^*}}{\sqrt{i_G^2 i_D^2}} = \frac{\overline{i_{G1} i_{D1}^*} + \overline{i_{G2} i_{D2}^*}}{\sqrt{i_G^2 i_D^2}} \tag{3.46}$$

First of all, the cross-correlation between channel noise and induced gate noise in Region I can be expressed by

$$\overline{i_{G1} i_{D1}^*} = \int_o^{V_C} \overline{\Delta i_{G1} \Delta i_{D1}^*} \Delta V = \int_o^{V_C} \overline{j\omega \Delta Q_1 \Delta i_{D1}^*} \Delta V \tag{3.47}$$

Inserting (3.34) into (3.47), then using (3.15) and (3.28) to carry out the integration, we obtain

$$\overline{i_{G1} i_{D1}^*} = j\omega \frac{4kT_0 \mu_{EFF} W_{EFF}^2 C_{OX}^2 M^2 \Delta f}{aR_O^2 I_D^3} \left(V_{GT} - aV_P \right) \times \left[P_C(1) - P_C\left(\frac{V_{GT}}{V_{GT} - aV_P} \right) \right] \tag{3.48}$$

where $P_C(\eta)$ is given in Appendix D. In (3.48), we have also employed the approximation given by (3.40) to simplify the integral calculation.

Similarly, we can evaluate the cross-correlation between channel noise and induced gate noise in Region II using (3.42). The result is

$$\overline{i_{G2}i_{D2}^{*}} = \overline{j\omega Q_2 i_{D2}^{*}} = j\omega \frac{\mu_{EFF} W_{EFF}^2 C_{OX}^2 \overline{i_{D2}^2}}{I_D^2} P_2 \tag{3.49}$$

Substituting (3.25) into (3.49), and employing (3.28), we then obtain

$$\overline{i_{G2}i_{D2}^{*}} = j\omega \frac{64qD\mu_{EFF} C_{OX}^2 W_{DC}^2 \Delta f}{\pi^5 \varepsilon_{Si}^2 v_{SAT}^3 x_{j,EFF} R_O^2 I_D} P_2 \left[\left(\frac{\pi L_2}{W_{DC}} \right) + 3 - 4\exp\left(\frac{\pi L_2}{2W_{DC}} \right) + \exp\left(\frac{\pi L_2}{W_{DC}} \right) \right] \tag{3.50}$$

Finally, using (3.48) and (3.50), the correlation coefficient C defined by (3.46) can be calculated. Its value is purely imaginary due to the fact that the gate noise and drain noise currents are coupling through the gate oxide capacitor.

3.4 Experimental Results and Model Validation

In this section, we verify the proposed DDN model with experimental data of the 120 nm CMOS technology in the frequency range of 2 to 26 GHz at different biasing conditions. The DUTs are n-channel MOSFETs which have the dimensions of W/L = 115 μm / 120 nm. The effective channel length, oxide thickness, effective junction depth and threshold voltage of the DUTs are determined to be L_{EFF} = 97 nm, t_{OX} = 2.5 nm, $x_{j,EFF}$ = 20 nm and V_T = 0.27 V, respectively. As mobile carriers in the DUTs are electrons, saturation velocity v_{SAT} of 8×10^6 cm/s and low-field mobility μ_0 of 360 cm^2/Vs were used to achieve best fitting results in the *I-V* characteristic. The selection of saturation velocity v_{SAT} is in agreement with published results in [38]. For noise simulation, we have set the high field diffusion coefficient and the hot electron temperature parameter to D = 20 cm^2/s and δ = 22, respectively. These values are within the range of the data reported in [39]-[40].

It is shown in Figure 3.2 that the measured power spectral density of drain noise S_{id} and induced gate noise S_{ig} are in excellent agreement with the modeled results at V_{DS} = 1.2 V and

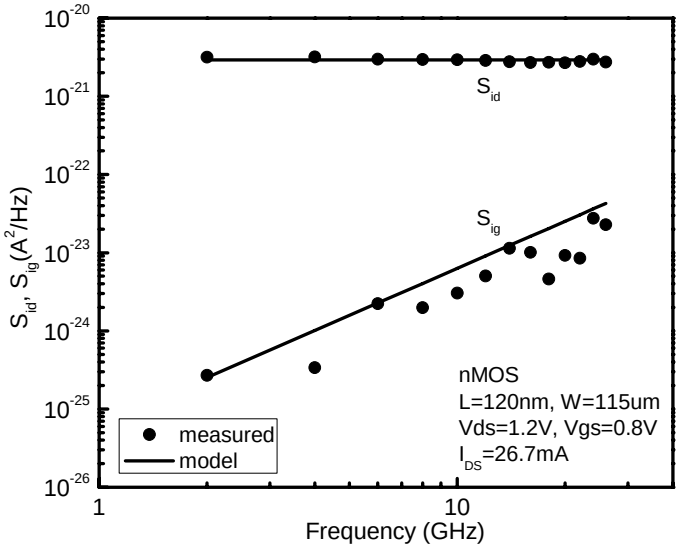
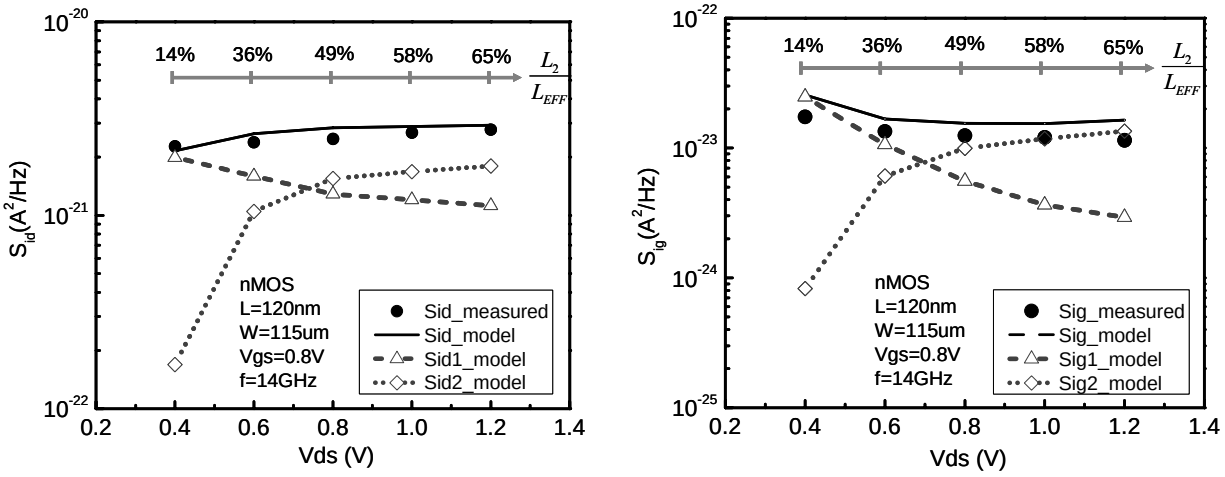


Figure 3.2: Measurement versus DDN model draine S_{id} and induced gate noise S_{ig} as a function of frequency in the range of 2 GHz to 26 GHz.

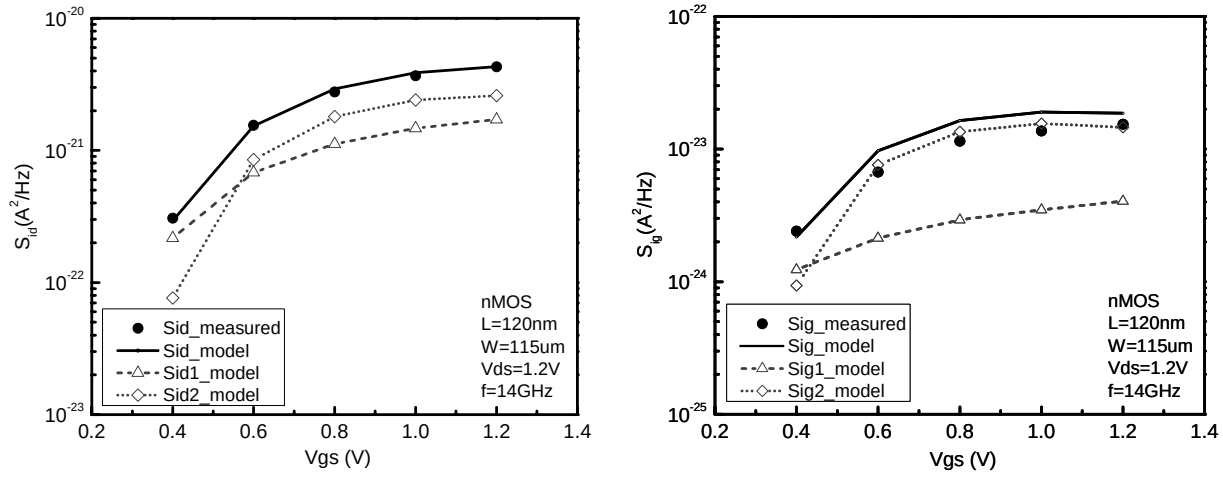
V_{GS} = 0.8 V over the frequency range of 2 to 26 GHz. Next, we investigate the dependences of the device noise sources on different biasing conditions. The results, including the total noise sources as well as regional noise contributions, are illustrated in Figures 3.3-3.4 at f = 14 GHz, the middle point of the measured frequency range. Again, the proposed DDN model shows accurate prediction of the measured data.

Furthermore, we observe an important feature that the noise generated from Region II actually becomes dominant at some biasing conditions. Figure 3.3 shows that when the drain voltage V_{DS} increases at a fixed gate voltage V_{GS}, the saturation length L_2 of Region II increases, and so does the noise contribution in this region. However, the total drain noise S_{id} as well as induced gate noise S_{ig} remains nearly constant due to the corresponding drop in noise contribution from Region I. If we keep V_{DS} fixed at high value and increase V_{GS}, the noise contributions of the two regions increase, which leads to the increment of both S_{id} and S_{ig} as shown in Figure 3.4. The device becomes noisier when it is driven at higher current density. At low V_{GS}, using only the noise source model from Region I, we can closely predict the measured



(a) (b)

Figure 3.3: Measurement versus DDN model: (a) drain noise S_{id} and (b) induced gate noise S_{ig} as functions of drain voltage V_{DS} for a fixed gate voltage V_{GS}.



(a) (b)

Figure 3.4: Measurement versus DDN model: (a) drain noise S_{id} and (b) induced gate noise S_{ig} as functions of gate voltage V_{GS} for a fixed drain voltage V_{DS}.

data. However, the discrepancy between experimental results and model predictions worsens as V_{GS} increases. The same observation has been reported by Scholten et al. [14] when considering noise sources only generated by Region I. Therefore, for nanometer MOSFETs under a high lateral field, the noise contribution from Region II plays an important role and cannot be

neglected.

Next, in Figure 3.5, we illustrate the measured versus modeled cross-correlation coefficient, C, between drain noise, $S_{id,}$ and induced gate noise S_{ig}. The corresponding noise correlations C_1 and C_2 from Region I and Region II are also plotted in Figure 3.5. As expected, the drain noise and induced gate noise due to noise sources in Region II are strongly correlated compared to the ones in Region I. The noise correlation C_1 of Region I has a shape similar to that of a long-channel MOSFET [41], while the noise correlation C_2 of Region II contributes to form a more general pattern of the total correlation C. At low V_{GS} and high V_{DS}, Region II can occupy a large portion of the device channel. However, its noise contribution is small due to low I_{DS}. Hence, C is also small at this bias level. When V_{GS} increases, (S_{id2}, S_{ig2}) become comparable to or even exceed (S_{id1}, S_{ig1}), as shown in Figure 3.4. As a result, C continues to increase to reach its peak. However, at high V_{GS}, Region II becomes smaller which will slow the increment of C and eventually lead to its drop. The data shown in Figure 3.5 is consistent

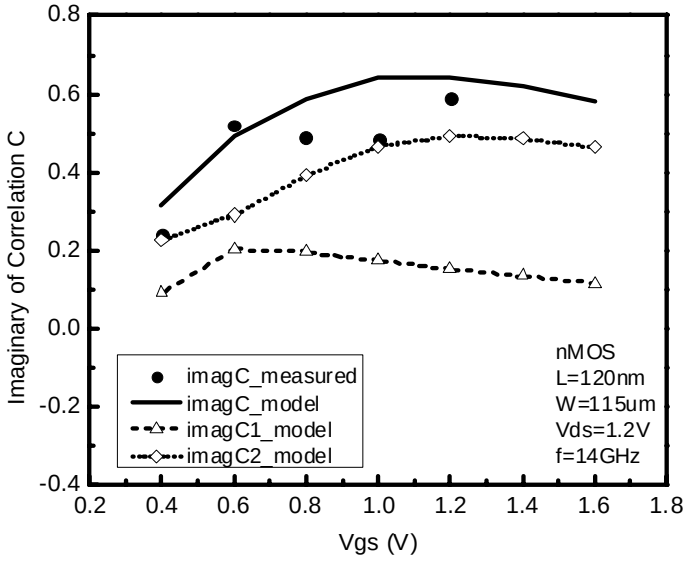


Figure 3.5: Measurement versus DDN model cross-correlation coefficient C as a function of gate voltage V_{GS} for a fixed drain voltage V_{DS}. C_1 and C_2 are the corresponding correlations from Region I and Region II, respectively.

with the results presented in [2] and [42]. In our experiments, to keep devices working under normal biasing conditions as specified by the process, we do not include the measured C at very high V_{GS} beyond 1.2 V.

To support RFIC design, we have incorporated the proposed DDN model with two noise sources into the BSIM3 compact model using sub-circuit techniques [43]. The DDN model shows excellent fitting results for the measured noise parameters of an n-MOSFET (L = 120 nm and W = 115 μm) at V_{DS} = 1.2 V and V_{GS} = 0.8 V in the frequency range of 2 to 26 GHz (Figure 3.6). As frequency increases, the effect of induced gate noise becomes more prominent and can no longer be ignored. The DDN model has taken into account these effects and show its superiority over the BSIM model with a strong enhancement in the noise prediction capability up to 1.2 dB for NF_{MIN} at 26 GHz (Figure 3.7). In addition, the model also accurately predicts the measured NF_{MIN} and associated gain G_A at different biasing conditions as shown in Figure 3.8.

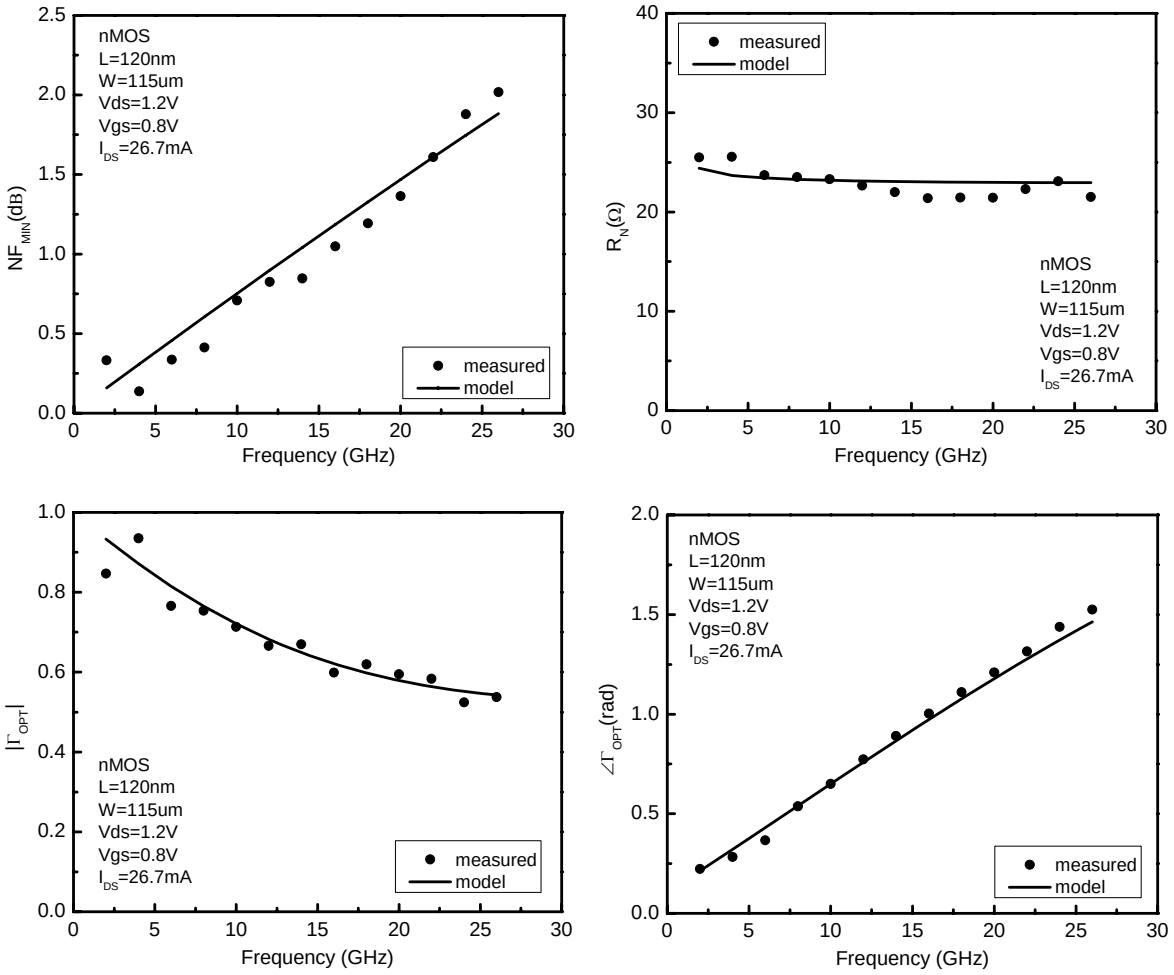


Figure 3.6: Measurement versus DDN model noise parameter of an n-MOSFET with L = 120 nm and W = 115 μm as a function of frequency in the range of 2 to 26 GHz at V_{DS} = 1.2 V and V_{GS} = 0.8 V.

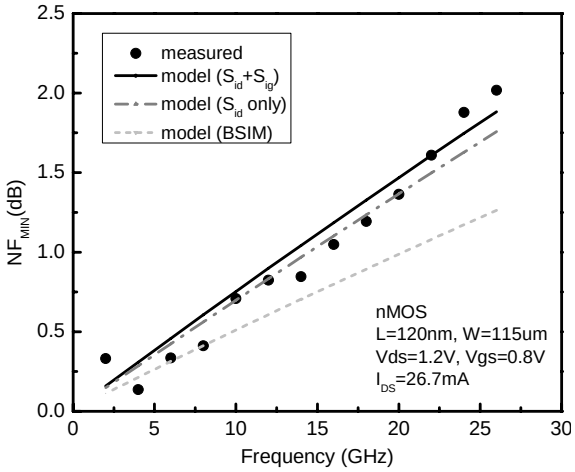


Figure 3.7: Comparison between DDN and BSIM noise models in predicting the minimum noise figure NF_{MIN} of an n-MOSFET with L = 120 nm and W = 115 μm. at V_{DS} = 1.2 V and V_{GS} = 0.8 V.

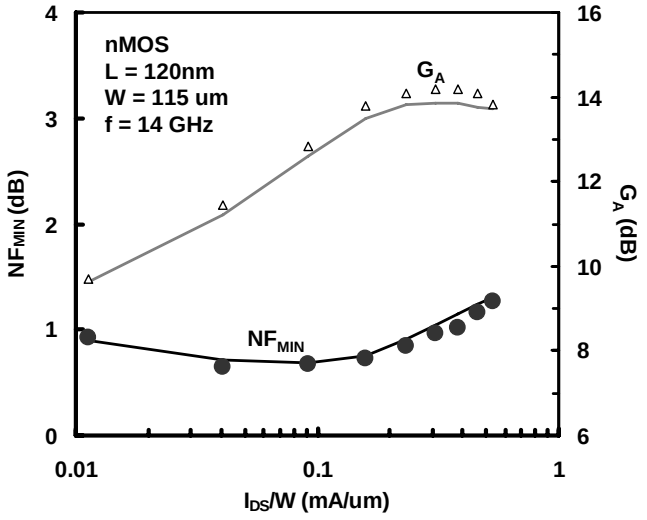
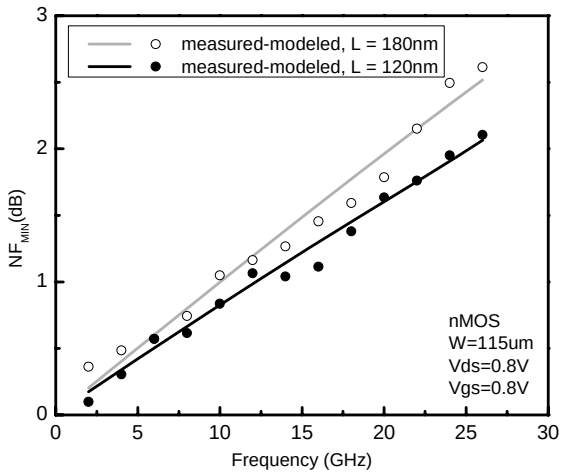
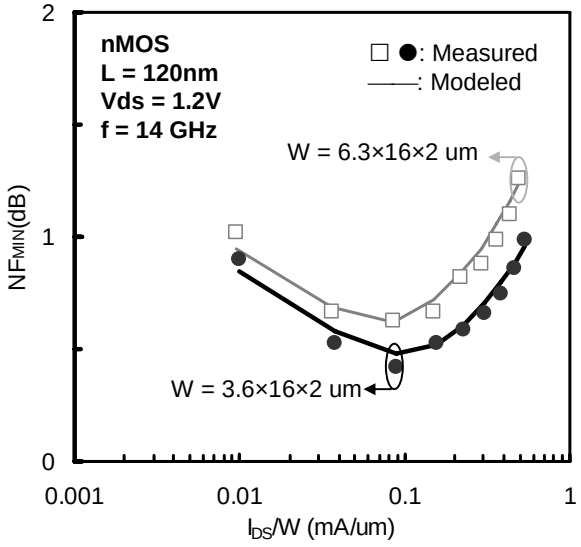


Figure 3.8: Measurement versus DDN model noise parameter of an n-MOSFET with L = 120 nm and W = 115 μm at 14 GHz for different bias current levels.

More important, as shown in Figure 3.9, the DDN model exhibits the ability to scale with gate length and width, which is crucial in integrated circuit design and optimization.



(a)



(b)

Figure 3.9: Scalability of the DDN model with gate length and width over different bias current levels.

4. A 3.1−10.6 GHz ULTRA−WIDEBAND LOW NOISE AMPLIFIER DESIGN

One of the testing circuits to verify the DDN model is the ultra-wideband (UWB) low noise amplifier (LNA). LNA is a critical circuit component in any modern wideband receiver. However, the designed circuit is not only used to validate the high-field MOSFET noise model developed in this work; it is also used to demonstrate the design improvement to achieve the lowest available noise level. The unique feature of the proposed technique is to use the Smith chart to design the input matching network to trade off between noise figure *NF* and input return loss (*RL* or $|S_{11}|$), a fundamental limitation on the design of LNAs.

4.1 Overview of UWB LNA Designs

Short-range wireless communication is becoming popular to replace cable-based systems due to its compact and high data rate connectivity. In the US, the FCC has approved a spectrum spanning from 3.1 to 10.6 GHz for low cost UWB systems with data rates that can reach 500 Mb/s. Such features have created the interest in designing new high performance circuits for potential UWB applications.

In an UWB system, the LNA must satisfy stringent requirements of low noise, high gain, and high return loss, as well as low power consumption over a very wide bandwidth. Moreover, the UWB LNA suffers many interferers from co-existing systems like WLAN and Bluetooth. This condition requires that the LNA linearity must be considered as important as its noise performance [44]. In recent literature, low noise performance is achieved using either noise and source impedance matching at the input [45]-[47] or noise cancelling techniques [48]. Typically, the MOSFET devices themselves have highly capacitive input impedances. Hence, by coupling with passive components in the form of source degeneration [46] or feedback [47]-

[48], it helps to generate the real part of the input impedance which can be matched to the 50 Ω source. Nevertheless, these approaches leave less freedom to optimize the gain cell to satisfy all the required parameters over a wide range of frequency. In the noise cancelling technique, the first stage is used to match to the source impedance, while noise cancelling is achieved by the following stages. This approach, however, still cannot satisfy both extremes, low *NF* and high IIP_3.

In this research, we present the design and implementation of a fully integrated UWB LNA in 120 nm CMOS process. The Smith chart is used to simultaneously match noise and source impedance. The gain cell is de-coupled from the input matching network to independently optimize its gain, noise, linearity and return loss. The LNA employs all triple-well nMOS devices. Figure 4.1 shows the RF parameters of such a device with the dimension of 0.12 μm x 190 μm. At 10 GHz, the minimum noise figure NF_{MIN} is less than 1 dB over the

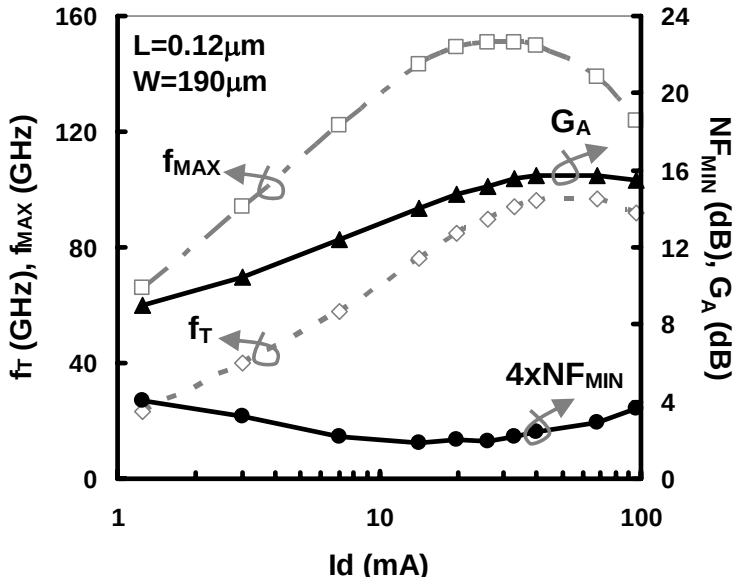


Figure 4.1: Measured NF_{MIN}, G_A (at f = 10 GHz) and f_T/f_{MAX} for a 0.12 μm x 190 μm triple-well nMOS device used in the LNA.

bias range up to 100 mA. However, there is no compromise between NF_{MIN} and associated gain G_A. Biased at 25 mA to obtain NF_{MIN}, the device shows associated gain G_A of 15 dB and f_T/f_{MAX} around 90 /150 GHz.

4.2 Circuit Design

4.2.1 Topology, device size and biasing

Cascode topology can help to reduce the effective input capacitance; hence, it is well suited to high gain and wide bandwidth amplifier design [49]. Since the *NF* of a MOSFET device decreases as the gate length decreases, all transistors in the cascode gain cell use minimum gate length available for the process, L=0.12 μm. However, as the device gate length decreases, its linearity worsens. To overcome this problem, the device needs to be biased at higher current density at the cost of increased power consumption [50]. In the cascode gain cell, the common source transistor (CST) is the dominant source of noise and distortion, so selection of the CST's width is crucial. To boost the gain of the cascode cell, the width of the CST is chosen as large as possible, which in turn increases its *NF*. Furthermore, larger device width will eventually exacerbate the distortion due to the effect of parasitic capacitances [51]. In this complicated context, measured data as well as simulation results were used to obtain the best solution. The circuit was simulated with Agilent Advanced Design System (ADS) using BSIM3v3 RF model enhanced by DDN noise model. Because the *NF* and the gain get worse as frequency increases, all the results are considered at 10 GHz, the upper end of UWB frequency band. The dimension of the CST is chosen to be 0.12 μm x 190 μm which takes into account all the described trade-offs of gain, noise and distortion. As shown in Figure 4.1, the CST is biased

at the current of 25 mA for low noise and low distortion operation. The overall noise and distortion performance of the circuit will degrade because of the common gate transistor (CGT). However, it is interesting to observe that the NF_{MIN} of the cascode cell varies with the width of the CGT. The corresponding width for minimum noise is found to be W_{CGT}=230 μm.

4.2.2 Input impedance and noise matching

The next design step is to match the cascode gain cell to the 50 Ω source impedance while keeping its NF as low as possible. Note that all the impedances (Z) can be represented by their corresponding reflection coefficients (Γ), and the *NF* described in (2.3) now can be re-expressed as

$$F = F_{MIN} + \frac{4r_n \left|\Gamma_S - \Gamma_{OPT}\right|^2}{\left(1-\left|\Gamma_S\right|^2\right)\left|1+\Gamma_{OPT}\right|^2}; \; NF = 10\log_{10}(F) \tag{4.1}$$

As the source reflection coefficient, Γ_S, reaches its optimum value (Γ_{OPT}), the noise figure *NF* reaches its minimum value of NF_{MIN}.

In general, the basic principle to design the input matching network can be described by Figure 4.2. $\Gamma_{IN,C}$ and $\Gamma_{OPT,C}$ are the input impedance and the optimum source reflection coefficient of the unmatched cascode gain cell, respectively. The input matching network is designed to transfer $\Gamma_{IN,C}$ to 50 Ω source impedance and convert this impedance to $\Gamma_{OPT,C}$. However, it is very challenging to fulfill the requirement over a large range of frequencies. This work proposes a graph-based technique to ease the design task while still achieving optimal matching requirements. Both $\Gamma_{IN,C}$ and $\Gamma_{OPT,C}$ are converted to the new values of Γ_{OPT} and Γ_{IN}, which are close to the 50 Ω to enable simultaneous matching. In practice, the matching networks also contribute noise, which results in higher NF_{MIN} for the combined gain and

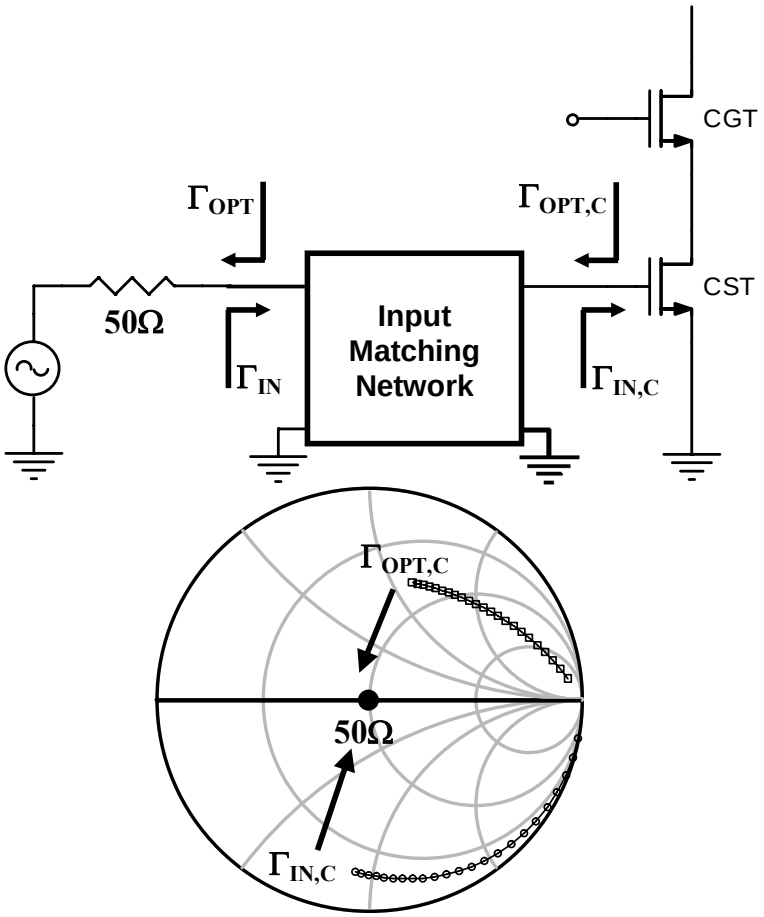


Figure 4.2: Basic principle for simultaneous source impedance and noise matching.

matching circuit. Hence, it is crucial to keep the matching network simple to reduce its noise contribution.

As shown in Figure 4.3, the $\Gamma_{IN,C}$ of the gain cell has highly capacitive reactance and low resistance over the design frequency range. In the first step, inductors L_1 and L_2 are used to cancel the imaginary part of $\Gamma_{IN,C}$ while resistor R_1 is necessary to increase its real part to 50 Ω. R_1 is also used to push $\Gamma_{OPT,C}$ toward the center point. The gate bias voltage of CST is fed through L_2. Because the goal is to match to the center point of the Smith chart, the second step employs an LC-section which includes L_3 and C_1 to roll off and tighten Γ'_{IN}. Finally, the inductor L_4 is used to move Γ'_{IN} and Γ'_{OPT} to their corresponding Γ_{IN} and Γ_{OPT} values which stay

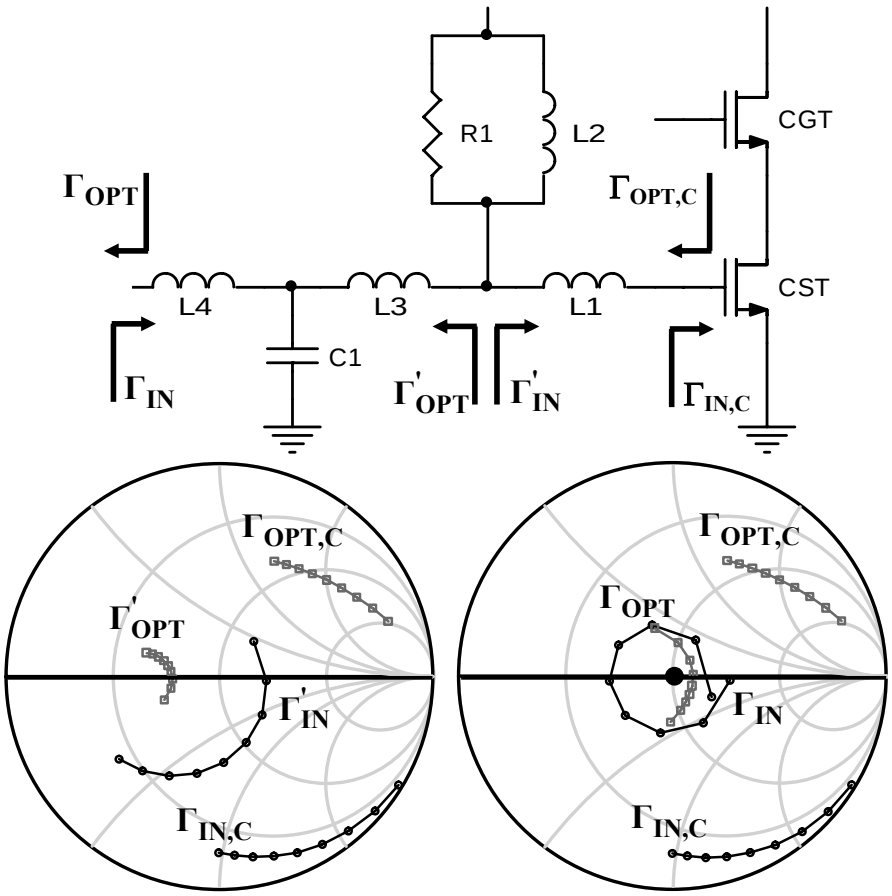


Figure 4.3: Proposed technique for simultaneous source impedance and noise matching in the frequency range 3-11GHz.

around the center point. The whole procedure is illustrated in Figure 4.3. The smaller the radius of the Γ_{IN} circle, the better the input *RL*.

4.2.3 Output matching and loading effects

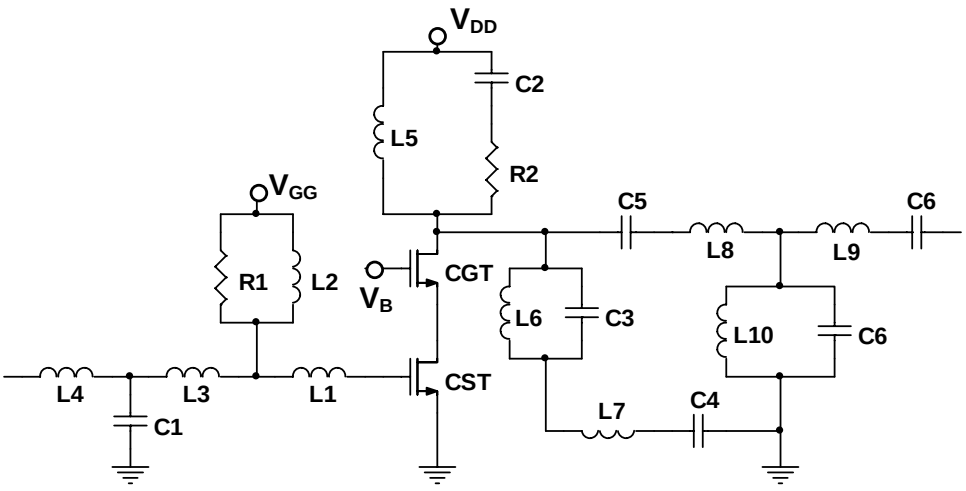
So far, most UWB LNA designs employ shunt-peaking load [52] to extend their bandwidth. However, the series resistance in the load can reduce the supply voltage, and hence the gain, of the active devices. In low voltage design, this effect is more significant. Therefore, an LC tuned load is proposed to overcome the problem. It is tuned to the mid-range frequency, which is around 6 GHz in the UWB band. The bandwidth is then widened by placing a resistor

in series with the capacitor of the tuned load. This resistor is also used to set the impedance at the output node, Z_{OUT}. In an integrated receiver, the LNA usually drives I/Q mixers which can be considered as capacitive loads, $Z_{C,LOAD}$. These loads strongly affect the LNA bandwidth. Therefore, an output matching network is essential to maintain the required bandwidth. In addition, the output matching network with very sharp cutoff frequency response also helps to attenuate any out-of-band blockers which can become stronger after passing through the gain cell. Using the image-parameter method [53], filters can be designed to satisfy both requirements. In this work, the output matching network is designed to match Z_{OUT} to 50 Ω for measurement purposes instead of $Z_{C,LOAD}$. The matching network is passive, so it does not consume any power as in the case of active buffers. The complete design of the LNA chip is shown in Figure 4.4.

4.3 Experimental Results

Fabricated in 120 nm CMOS process, the prototype UWB LNA chip occupies a compact area of 0.95x0.72 mm including RF and DC pads. High frequency on-wafer measurements are carried out using ATN-NP5B automated noise figure measurement system. Collected data is then de-embedded using an "Open" and "Short" technique to remove effects of the RF pads and interconnection as described in Chapter 2.

As shown in Figure 4.5, the amplifier achieves a 3 dB bandwidth from 2.75 to 10.1 GHz with maximum gain of 12.76 dB. Its corresponding *NF* at 50 Ω source impedance (NF_{50}) is varied between 3.52 dB and 4.3 dB, and input *RL* is better than 9 dB. The measured noise data matches pretty well with simulation results, validating the proposed DDN noise model. The output matching network is designed to have a very sharp cut-off response which can reduce



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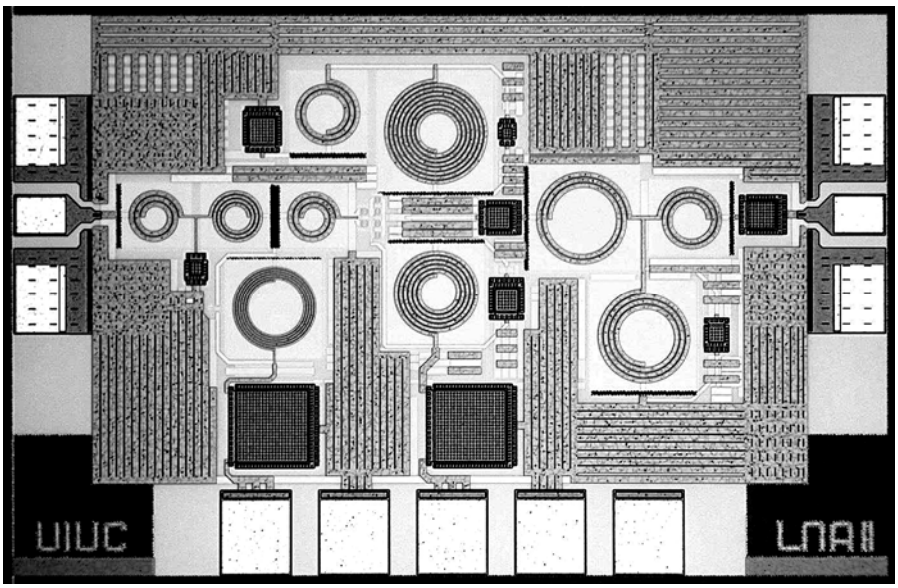


(b)

Figure 4.4: (a) Schematic and (b) microphotograph of the designed UWB LNA.

the gain to 0 dB only 1 GHz away from its -3 dB frequency. This explains why the out-of-band NF_{50} increases rapidly. The two-tone third-order intercept point is also measured to identify the linearity of the amplifier. Both Agilent 83651B and 8364A are used to provide highly pure sinusoidal RF signals. The two tones with 2 MHz spacing are combined and applied to the

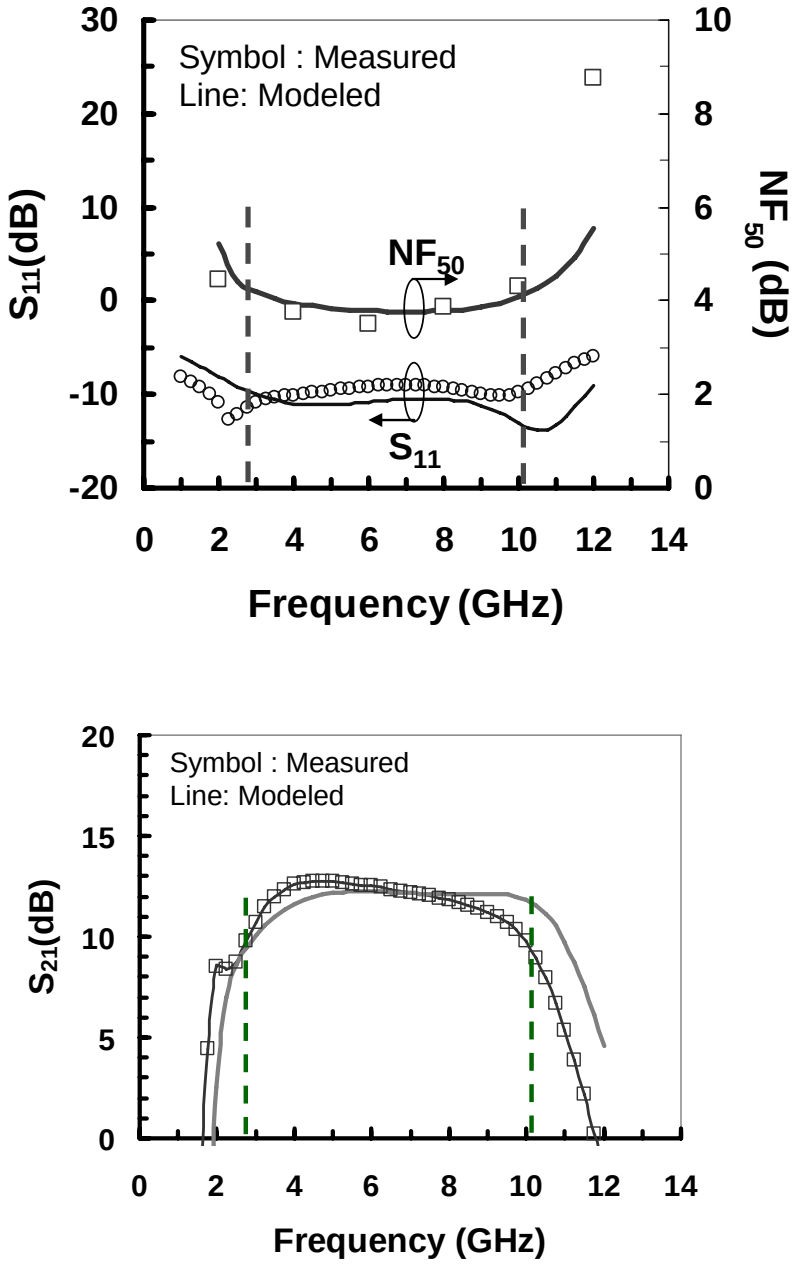


Figure 4.5: Measured versus simulated RF performance of the UWB LNA: (a) Noise figure at 50Ω source impedance (NF_{50}) and input return loss S_{11}, (b) gain S_{21}.

LNA. At 6 GHz, the measured *IIP3* is found to be 3.5 dBm. Across the bandwidth, the *IIP3* decreases from 5.2 dBm at 2GHz to 3.5 dBm at 10 GHz (see Figure 4.6). For a robust UWB receiver, an *IIP3* on the order of -9 dBm is essential [44]. Therefore, when integrated with a 5 dBm *IIP3* mixer, a 12 dB gain LNA needs to have an *IIP3* greater than -5 dBm. If the LNA has

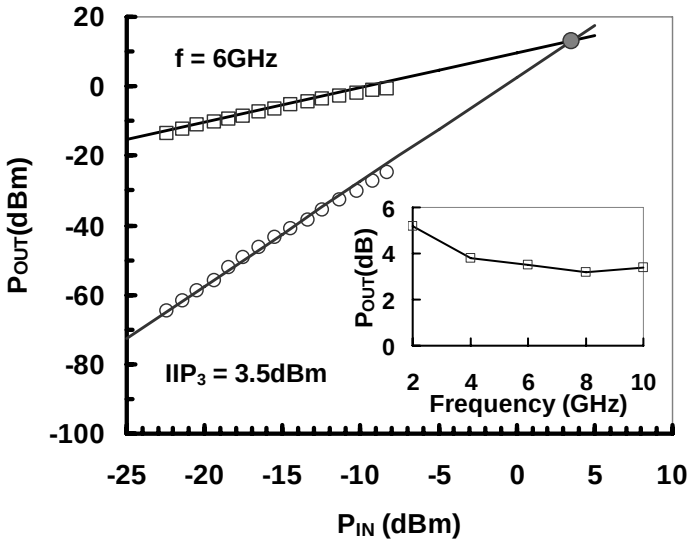


Figure 4.6: Linearity measurement of the UWB LNA.

higher gain and the mixer is less linear, this requirement is even more stringent. With *IIP3* better than 3.5 dBm over the bandwidth, the designed LNA can satisfy even the toughest linearity requirements while relaxing the design of the I/Q mixer. The linearity efficiency of the LNA, which is defined by $IIP3/P_{DC}$, is also better than those of other reported designs.

The measured performance of the LNA is summarized in Table 4.1. The amplifier achieves very low NF and its linearity is superior. Moreover, the overall performance in terms of gain, noise, linearity and input return loss are excellent in comparison to other designs. This proves the effectiveness of the proposed design methodology and the accuracy of the DDN as well.

Table 4.1 Performance summary and comparison with previous published works

Reference	CMOS Tech.	G_{MAX} (dB)	BW (GHz)	NF_{50} (dB)	$\|S_{11}\|$ (dB)	IIP_3 (dBm)	P_{DC} (mW)	Area (mm^2)
Bevilacqua JSSC 2004 [45]	0.18 μm	10.4	2.4 - 9.5	4.2 - 8	> 9.4	< -8	18	1.1
Reiha JSSC 2007 [46]	0.13 μm	16.5	1.74 - 10.7	2.1 - 2.9	> 9.9	< -5.1	9	0.87
Jung MOTL 2007 [47]	0.18 μm	13.5	1.85 - 10.2	4.1 - 5.7	> 10	< -1	13	0.63
Liao JSSC 2007 [48]	0.18 μm	9.7	1.2 - 11.9	4.5 - 5.1	> 11	< -4.9	29	0.59
This work RFIC 2008	0.13 μm	12.76	2.75 – 10.1	3.5 - 4.3	> 9	< 5	30	0.68

5. A 24 GHz LOW NOISE AMPLIFIER DESIGN

This chapter presents the design of an RF CMOS LNA for 24 GHz industrial, scientific, and medical (ISM) applications. The design employs a coplanar waveguide (CPW) structure as series feedback to achieve simultaneous noise and power matching. As the application frequency goes beyond 10 GHz, the task is effectively assisted by the advanced DDN model to enable first-pass silicon design.

5.1 Overview of 24 GHz ISM Band LNA Designs

Due to the overcrowded transmission in the frequency bands below 10 GHz as well as the high demand for multi-gigabit-per-second data rates for wireless communication, the Federal Communications Commission (FCC) has opened the 24-24.25 GHz unlicensed band for ISM applications. Although III-V processes still dominate the area of high frequency designs, scaled CMOS technology has the potential to build circuits operating beyond 20 GHz [54]. This advance, together with the capability to provide low cost and high integration solutions, has accelerated the research on CMOS monolithic microwave integrated circuits (MMICs).

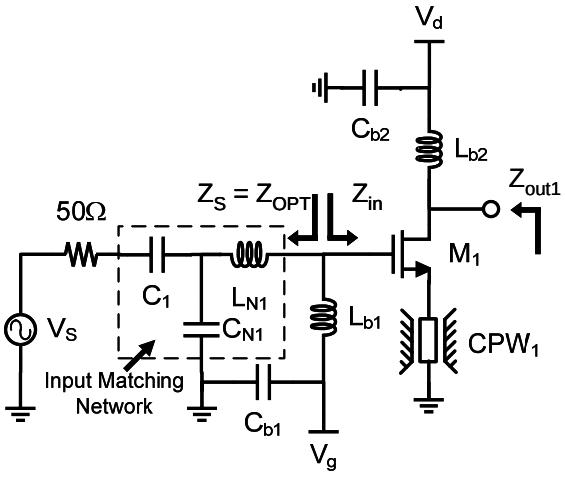
LNAs are key circuit components in any RF front-end. To design CMOS LNAs with noise and gain performance comparable to III-V LNAs is still very challenging. Recent reports on 24 GHz LNA design [55]–[57] typically use common-source and inductive degeneration techniques to achieve both noise and power matching. This technique simplifies the design of the input matching network and reduces its noise contribution to the overall amplifier. However, the constrained selection of the source degeneration inductance to match the device input impedance to 50 Ω source impedance can also lead to degradation of the circuit gain.

Moreover, MOSFETs are considered bilateral devices at microwave frequencies, and the gate-to-drain capacitance, C_{GD}, cannot be ignored as is done in the literature. In [54], the common-gate topology with resistive feed-through is introduced as an alternative for circuits operating at these frequencies. Nevertheless, with an *NF* of 6 dB, the prototype still cannot outperform the common-source configuration with inductive degeneration [55] – [57], though it does exhibit higher gain.

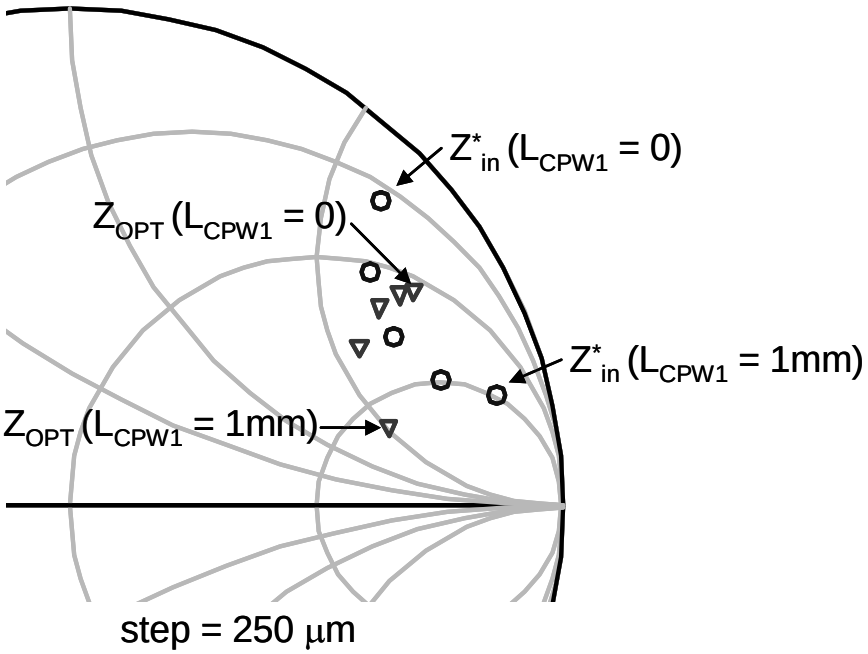
In this chapter, a fully integrated 24 GHz CMOS LNA with a *NF* of 3.8 dB and a gain of 19 dB is demonstrated. The LNA shows the highest gain to date in the 24 GHz band while maintaining a competitive *NF*. The circuit is achieved by using our accurate DDN model, which is able to predict the noise behavior of nanometer MOSFETs up to 26 GHz. In addition, the LNA employs on-chip CPW in series feedback to bring its optimum source impedance and conjugate input impedance in close proximity, such that simultaneous noise and power matching can be achieved for a given load impedance. Since the length of the CPW is not strictly constrained in the design, and its equivalent inductance is very small, on the order of pH, the LNA can thus achieve high gain.

5.2 Circuit Design

Since it is quite challenging to build a standard CMOS LNA at 24 GHz to compete with a III-V LNA, say, with 2 dB *NF* and 20 dB gain, a divide-and-conquer two-stage topology is selected for this design with a power budget of 20 mW. The first stage uses a common-source topology to achieve low-noise performance ($NF \approx 2$ dB, gain ≈ 6 dB), while the second stage adopts a cascode configuration to deliver gain ($NF \approx 4$ dB, gain > 9 dB). Since the NF_{MIN} of a MOSFET decreases with its gate length, all transistors in the LNA are chosen to have the



(a)



(b)

Figure 5.1: (a) First stage common-source amplifier employing CPW as series feedback. (b) Effect of the CPW_1 (step $\triangle L_{CPW}$ = 250 μm) on the optimum source impedance Z_{opt} for NF_{MIN} and the conjugate of input impedance Z^*_{in} for power matching.

minimum length available in the process. In addition, as shown in Figure 3.6, NF_{MIN} is also a function of device width. As a result, to keep NF_{MIN} low while achieving the required gain, the total width of the first-stage transistor M1 is chosen to be 38.4 μm with 16 fingers. As shown in Figure 5.1 (a), the gate and drain bias of M1 are established by two integrated biasing networks

(Lb1, Cb1) and (Lb2, Cb2), respectively. With a 5.5 mA drain current, M1 demonstrates a cut-off frequency f_T of 80 GHz and a maximum oscillation frequency f_{MAX} of 100 GHz. As described by (4.1), the best noise performance ($NF = NF_{MIN}$) occurs when the source impedance Z_S equals to the optimum value Z_{OPT} of the unmatched device. Meanwhile, the power matching happens when Z_S is equal to the conjugate of the device input impedance Z^*_{in}. Unfortunately, Z_{OPT} is typically different from Z^*_{in}. To bring these values in close proximity to each other, we introduce a CPW as series feedback to the unmatched device (Figure 5.1) at the cost of increasing the achievable NF_{MIN} and reducing the gain slightly. Using the DDN model, the accurate values of Z_{OPT} are obtained as the length of the series-feedback CPW_1 are varied, and the optimum value of CPW_1 for $Z_{OPT} \sim Z^*_{in}$ is found to be 270 μm as shown on the Smith chart in Figure 5.1 (b). A simple series-shunt LC section [58] is then designed to convert Z_{OPT} to the source impedance of 50Ω. The topology (L_{N1}, C_{N1}) in Figure 5.1 (a) is selected by considering its noise contribution as well as the practical aspects of implementation. To reduce the noise contribution from the biasing network, both L_{b1} and L_{b2} in Figure 5.1 (a) are designed to have a high quality factor Q. As L_{b2} is also the load of M1, its value is selected to push the unmatched device to reach the highest gain available at 24 GHz. In Figure 5.1 (a), C_1 is the input DC-blocking capacitor.

The second stage is a cascode amplifier with CPW series feedback as well. To achieve high gain, the width of the common-source transistor is chosen to be 57.6 μm to derive enough gm, while the width of the cascode transistor is optimized at 76.8 μm to minimize its noise contribution. The second stage is biased at 7 mA drain current to meet the power budget while delivering enough gain and low *NF*. To achieve maximum power transfer from the first stage to the second, an inter-stage matching network is necessary. In this design, the second-stage input

impedance Z_{in2} is directly transformed to the conjugate of the first-stage output impedance Z^*_{out1} by the matching network of (C_{N2}, L_{N2}, L_{N3}), which is chosen to meet the design goal while considering device sizes, noise contribution, and practical component values for implementation. The capacitor C_2 is needed to block the DC path formed by the two inductors L_{N2} and L_{N3}. Lastly, a shunt-series LC section (L_{N4}, C_{N3}) is used to match the conjugate of the second-stage output impedance Z^*_{out2} to 50 Ω. Another capacitor C_3 is necessary for output DC-blocking. In this design, lumped components for the LC sections are used to reduce chip size, since the wavelength is still too long, on the order of several millimeters, at 24 GHz to use transmission lines. The complete schematic of the LNA and its microphotograph are shown in Figure 5.2 and Figure 5.3, respectively.

5.3 Experimental Results

Fabricated in a 120 nm CMOS process, the prototype LNA occupies a silicon area of 0.85 × 0.66 mm^2. High frequency on-wafer measurements were carried out using an ATN−NP5B automated noise-figure measurement system. Although the ATN−NP5B system can measure both noise and S-parameters at the same time, it can only measure up to the frequency of 26 GHz. To show values at higher frequencies, the small-signal gain and return losses of the LNA were measured separately using Agilent 8364A PNA.

As shown in Figure 5.4, the LNA achieves gain of 19 dB, *NF* of 3.8 dB, and input/output return losses (RL) $|S_{11}|$ and $|S_{22}|$ of 9.5 dB and 15 dB, respectively, at 24 GHz. Across the 24.0-24.25 GHz ISM band, the gain was measured at better than 18.5 dB, and the *NF* was lower than 4 dB. The measured -3 dB bandwidth of the two-stage LNA is from 21 to 25 GHz. The total power consumption is 15 mW from a single 1.2 V power supply. In addition,

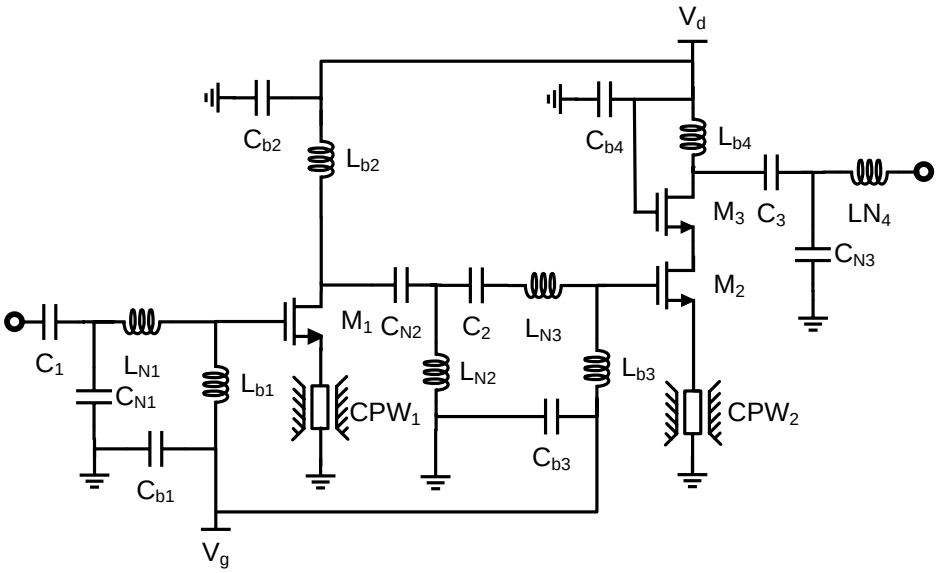


Figure 5.2: Schematic of the two-stage 24 GHz CMOS LNA.

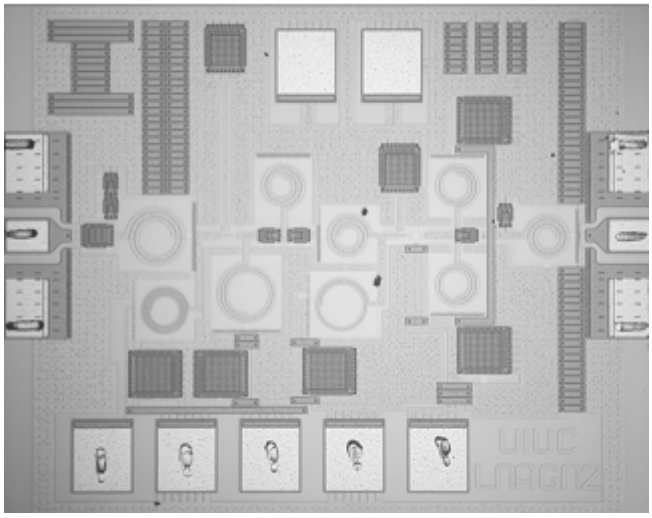


Figure 5.3: Die photo of the 24 GHz CMOS LNA with a chip size of 0.85 × 0.66 mm^2.

the linearity of the LNA was also characterized. The measured input-referred 1 dB compression point (P1-dB,in) was -17.9 dBm under the same test condition as in the gain and NF measurements (Figure 5.5), with an output power of 0.14 dBm, i.e., the P1-dB,out.

In Figure 5.4, the better agreement between measurement and simulation using the DDN model as compared to that using the BSIM3 model reveals the superiority of the DDN model in predicting the noise performance of nanometer MOSFETs. The shifted peak gain of

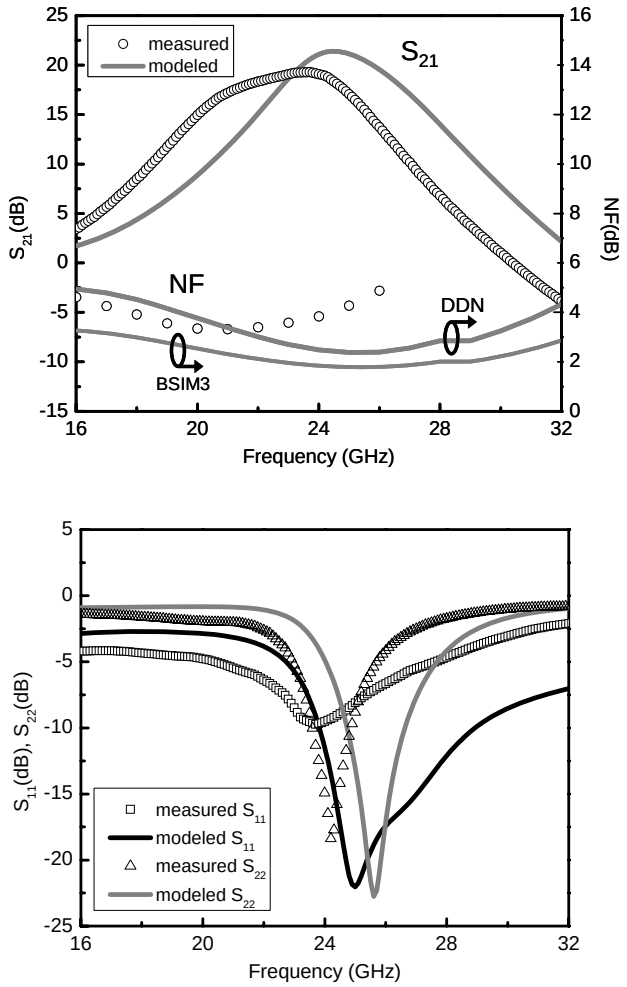


Figure 5.4: Measured versus modeled noise figure *NF* and S-parameters of the 24 GHz CMOS LNA.

the LNA in measurement is largely due to unaccounted-for parasitics and their effect on the chip operation at 24 GHz. The performance of the LNA is summarized in Table 5.1 with comparison to previous published works. To the best of our knowledge, this LNA achieves the highest gain to date in the 24 GHz band with a competitive NF and reasonable power consumption.

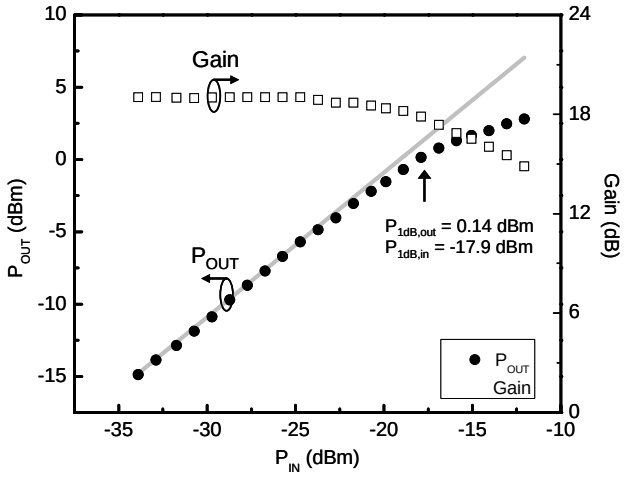


Figure 5.5: Measured 1 dB compression point of the 24 GHz CMOS LNA.

Table 5.1 Performance summary and comparison with previous published works

	This work	[55] RFIC05	[56] MWCL05	[57] RFIC08
Technology	130 nm CMOS	130 nm CMOS	180 nm CMOS	180 nm CMOS
f_T/f_{MAX} [GHz]	80/100	85/90	70/58	N/A
Peak gain freq. [GHz]	24	21	24	24
Gain [dB]	19	12.9	13.1	12.8
NF [dB]	3.8	5.2	3.9	3.3
Input/Output RLs [dB]	9.5/15	13/20	15/20	7.5/17
Power Consumption [mW]	15	16.8	14	8
Chip size [mm^2]	0.56	0.31	0.34	0.55

6. CONCLUSIONS

In this thesis, a high-field noise model (DDN) for nanometer MOSFETs working at saturation that predicts both channel and induced gate noise at high frequency is developed based on Statz's drifting-dipole theory. The model is able to accurately predict RF noise data of 120 nm MOSFETs under various bias conditions in the frequency range from 2 to 26 GHz. In addition, the scalability of the model with device size makes it useful for RFIC designs. More important, we found that the noise generated by the high-field region cannot be neglected; indeed, it plays an important role in determining the noise behavior of nanometer MOSFETs. The analytical formulations of the proposed model make it easy to integrate in circuit simulators like ADS or Spectre using Verilog-A scripts.

Two fully integrated LNAs designed for high-speed data communications in the frequency range of 3.1−10.6 GHz and 24 GHz have been demonstrated. Graph-based techniques using the Smith chart are employed to achieve simultaneous noise and power matching. The advanced DDN model developed in this work is extensively used to provide insights into and guidance for the designs. Measured results show the LNA chips achieve high performance in terms of noise figure, gain and linearity across the bandwidth, which can be extended to state-of-the-art designs. The simulation results of the designed circuits are in excellent agreement with measured data, and hence validate the proposed high-field noise model at the integrated circuit level up to 26 GHz.

Future work will primarily focus on extending the study results in thesis to technologies beyond 90 nm CMOS. As the technology aggressively scales down to 10 nm, the high-field region in the device can occupy up to 90% of the whole MOSFET channel, and hence the high-field noise source is expected to be dominant. In addition, the induced gate noise is also shown

to play an important role in the DDN model at higher frequencies approaching the millimeter wave region. Therefore, V-band or W-band LNAs should be designed and fabricated to verify the accuracy of the proposed DDN model.

APPENDIX A

DERIVATION OF ΔV_{D1} AS A FUNCTION OF ΔV_1

In this appendix, we derive the open-circuit noise voltage at the drain terminal ΔV_{D1} due to thermal noise ΔV_1 generated by an infinitesimal section in Region I. Since the drain fluctuation current is zero under the assumed open-circuit drain conditions, taking the differentiation of I_D in (2.10) and neglecting second-order terms, we then obtain

$$\Delta I_D = -a\Delta V_1 dV + \left(V_{GT} - aV\right) d\left(\Delta V_1\right) = 0 \tag{A.1}$$

$$\frac{d\left(\Delta V_1\right)}{\Delta V_1} = \frac{adV}{\left(V_{GT} - aV\right)} \tag{A.2}$$

Integrating (A.2) over the length of Region I, the noise voltage at the critical point ΔV_C due to ΔV_1 is thus seen by

$$\Delta V_C = \frac{V_{GT} - aV}{V_{GT} - aV_C}\Delta V_1 \tag{A.3}$$

Since the drain current I_D is kept constant, the critical voltage V_C also does not change its value. Therefore, the noise fluctuation at the critical point ΔV_C can only vary the length of both Region I and Region II such that

$$\Delta V_C = E_C \Delta L_1 = -E_C \Delta L_2 \tag{A.4}$$

This kind of noise-induced channel length modulation eventually results in the drain voltage fluctuation which can be obtained by differentiating (3.7)

$$\Delta V_{D1} = M\Delta V_C \tag{A.5}$$

where M is a hyperbolic function shown by

$$M = \cosh\left(\frac{\pi L_2}{2W_{DC}}\right) \Bigg/ \left[1 - \left(\frac{2\gamma_0 W_{DC}}{\pi L_{EFF}}\right)\sinh\left(\frac{\pi L_2}{2W_{DC}}\right)\right] \tag{A.6}$$

The function M is always greater than 1, so thermal noise generated by Region I is enhanced at the drain terminal. As expected, $M = 1$ when $L_2 = 0$. Substituting (A.3) into (A.5), we obtain (3.14) of the text.

APPENDIX B

DRIFTING DIPOLE POTENTIAL DIFFERENCE

The potential distribution due to a charge dipole is calculated in this section. As described in Figure B.1, a charge sheet of density $\sigma = q/A$ spreading from $y = 0$ to $y = W_1$ and put on top of a ground plane at $y = W_2$ has a potential expressed in general space-harmonic form by

$$\Phi(x,y) = \sum_{k=1,3,5\ldots}^{\infty} a_n \cos\left(\frac{k\pi y}{2W_2}\right)\exp\left[-\frac{k\pi(x-x_0)}{2W_2}\right] \tag{B.1}$$

The potential $\Phi(x,y)$ satisfies the following boundary conditions:

$$\Phi(x,W_2) = 0 \tag{B.2}$$

$$E_x(x_0,y) = \frac{\partial\Phi(x_0,y)}{\partial x} = \frac{\sigma}{2\varepsilon_{Si}} \tag{B.3}$$

The first condition is satisfied by choosing the functions representing $\Phi(x,y)$ while the second condition can be solved for a_n using Fourier expansion, as seen by

$$a_n = -\left(\frac{\sigma}{\varepsilon_{Si}W_2}\right)\left(\frac{2W_2}{n\pi}\right)^2 \sin\left(\frac{k\pi W_1}{2W_2}\right) \tag{B.4}$$

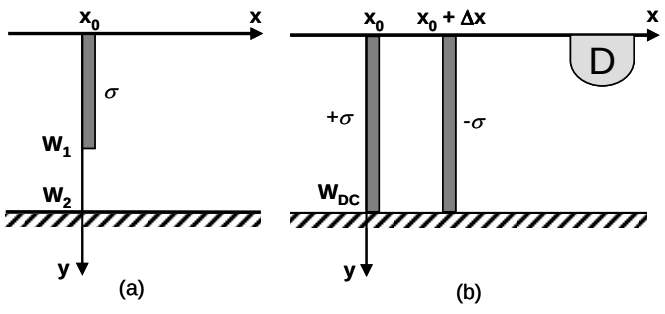


Figure B.1: (a) A charge sheet on top of a ground plane. (b) Drifting dipole formed in high field Region II.

For the MOSFET case shown in Figure B.1, we have assumed the mobile carriers drifting through Region II are confined within the depletion width, $W_1 = W_2 = W_{DC}$, and hence the potential of the charge sheet now becomes

$$\Phi(x,y) = \sum_{k=1,3,5...}^{\infty} -\left(\frac{\sigma}{\varepsilon_{Si} W_{DC}}\right)\left(\frac{2W_{DC}}{k\pi}\right)^2 \cos\left(\frac{k\pi y}{2W_{DC}}\right) \times \exp\left[-\frac{k\pi(x-x_0)}{2W_{DC}}\right] \qquad \text{(B.5)}$$

Next, the dipole potential difference can be calculated by differentiation of (B.5), as seen by

$$\Psi_{DP}(x,y) = -\frac{\partial\Phi(x,y)}{\partial x}\Delta x_0 = \sum_{k=1,3,5...}^{\infty}\left(-\frac{2\sigma}{k\pi\varepsilon_{Si}}\right)\cos\left(\frac{k\pi y}{2W_2}\right)\exp\left[-\frac{k\pi(x-x_0)}{2W_2}\right]\Delta x_0 \qquad \text{(B.6)}$$

If we approximate the results to the lowest order term and consider the potential difference distribution for both cases $x > x_0$ and $x < x_0$, we finally obtain (3.18) in the text.

APPENDIX C

DERIVATION OF ΔV_1 AND Δi_{D1} RELATION

Under short-circuit drain condition, the appearance of any noise voltage ΔV_1 in Region I results in a drain current fluctuation Δi_{D1}. Applying the *I-V* relation given in (3.10), then

$$I_D + \Delta i_{D1} = f\left(V + \Delta V_1\right) \frac{d\left(V + \Delta V_1\right)/dx'}{1 + \left(1/E_C\right) d\left(V + \Delta V_1\right)/dx'} \tag{C.1}$$

where the function *f* is defined by

$$f\left(V\right) = \mu_{EFF} W_{EFF} C_{OX} \left(V_{GT} - V\right) \tag{C.2}$$

Taking the perturbation of *f,* one obtains

$$f\left(V + \Delta V_1\right) = \frac{df\left(V\right)}{dV} \Delta V_1 + f\left(V\right) \tag{C.3}$$

Substituting (C.3) into (C.1) and neglecting high order terms lead to the differential equation

$$\Delta i_{D1} = \frac{d}{dx}\left[f\left(V\right) \Delta V_1 - \frac{\Delta i_{D1}}{E_C} V \right] \tag{C.4}$$

The solution of (C.4) is (3.32) of the text, which satisfies the conditions $\Delta V_1 = 0$ at $x = 0$, and $\Delta V_1 = 0$ at $x = L_1 = L_{EFF}$. The coefficient ζ in (2.32) is employed to account for the fact that if $L_1 \neq L_{EFF}$, then it is not necessary that $\Delta V_1 = 0$ at the end of Region I. At $x = x_0$, from (3.32), the potential discontinuity is given by

$$\Delta V_1 = -\frac{\zeta\left(L_1 + V/E_C\right)}{f\left(V\right)} \Delta i_{D1} \tag{C.5}$$

Then, the coefficient ζ can be determined by substituting (3.14) into (C.5) and considering $\Delta i_{D1} = \Delta V_{D1}/R_O$ under short-circuit conditions, as seen by

$$\zeta = -\frac{R_O f\left(V_C\right)}{M\left(V_C/E_C + L_1\right)} \tag{C.6}$$

APPENDIX D

DERIVATION OF $P_G(\lambda)$ AND $P_C(\eta)$

From the integration of (2.38), we derive the quantity $P_G(\lambda)$ in (3.39). The result is

$$P_G(\lambda) = a_7\lambda^7 + a_5\lambda^5 + a_4\lambda^4 + a_3\lambda^3 + a_2\lambda^2 + a_1\lambda + a_{01}\ln(2\lambda - 1) + a_{02}(2\lambda - 1) \qquad \text{(D.1)}$$

where the coefficients a_i are given by

$$\begin{aligned}
a_7 &= P_1^2/112 \\
a_5 &= (P_1/80)\left[-8P_0 + (\delta + 24)(P_1/4)\right] \\
a_4 &= \delta\left(P_1^2/256\right) \\
a_3 &= P_0^2/3 - (\delta + 12)(P_0P_1/24) + (9/768)(3\delta + 16)P_1^2 \\
a_2 &= (\delta/16)\left[-P_0P_1 + (13/16)P_1^2\right] \\
a_1 &= (\delta/64)\left[16P_0^2 - 30P_0P_1 + (221/16)P_1^2\right] \\
a_{01} &= (\delta/64)\left[16P_0^2 - 28P_0P_1 + (195/16)P_1^2\right] \\
a_{02} &= -(\delta/128)\left[4P_0 - (13/4)P_1\right]^2
\end{aligned}$$

From the integration of (2.47), we derive the quantity $P_C(\eta)$ in (3.48). The result is

$$P_C(\eta) = a_7\eta^7 + a_5\eta^5 + a_4\eta^4 + a_3\eta^3 + a_2\eta^2 + a_1\eta + b_{01}\ln(2\eta - 1) + b_{02}(2\eta - 1) \qquad \text{(D.2)}$$

where the coefficients b_i are given by

$$\begin{aligned}
b_5 &= -P_1/20 \\
b_3 &= P_0/3 - (\delta + 12)(P_1/48) \\
b_2 &= -\delta P_1/32 \\
b_1 &= (\delta/16)\left[4P_0 - (15/4)P_1\right] \\
b_{01} &= (\delta/8)\left[2P_0 - (7/4)P_1\right] \\
b_{02} &= (\delta/32)\left[-4P_0 + (13/4)P_1\right]
\end{aligned}$$

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